ADC Testing Using Digital Stimuli

Xiaoqin Sheng

ADC TESTING USING DIGITAL STIMULI

Xiaoqin Sheng

Composition of the PhD dissertation committee:

Prof.dr.ir. A.J. Mouthaan	Universiteit Twente (voorzitter en secretaris)
Prof. dr. ir. G.J.M. Smit	Universiteit Twente, NL (promotor)
Dr. ir. H.G. Kerkhoff	Universiteit Twente, NL (assistant-promotor)
Prof. dr. J.L. Hurink	Universiteit Twente, NL (intern lid)
Prof. ir. A.J.M. van Tuijl	Universiteit Twente, NL (intern lid)
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Prof. dr. A. Richardson	University of Lancaster, GB (extern lid)
Dr. A.C. Kruseman	NXP Semiconductors (referent)

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Xiaoqin Sheng

born on 4th of June 1981,
in Wuhan, China

This dissertation is approved by

Prof.dr.ir. G.J.M. Smit	University of Twente (promotor)
Dr.ir. H.G. Kerkhoff	University of Twente (assistant-promotor)

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Chapter 1

Introduction

1.1 Introduction

Nowadays, the products from semiconductor industry are everywhere in people's daily life, for example, TVs, mobile phones, digital cameras, computers and so on. Every day, a huge amount of integrated circuits (ICs) are being fabricated, which create considerable business profit. In 2007, the global revenues of the semiconductor industry were about USD 260 billion [ITR09]. The large demand of ICs drives the semiconductor technology development, resulting in increased IC performance and transistor counts per IC. As a result, semiconductor test technology requirements are also pushed to higher limits.

Production testing plays a very important role in semiconductor industry. Its main function is to guarantees that only IC products of good quality are delivered to the customers. The cost of production test is a large fraction of the total cost of the IC products. It requires test equipment, device interface boards (DIB), test engineers and test time, all of which should be counted in the test cost [Bur00]. Decreasing the test cost is continuously demanded by the IC industry. This demand drives a lot of research work being carried out on testing.

In semiconductor products, a system-on-chip (SoC) is a very popular type of IC. It

integrates an electronic system on one single chip. It is widely used in communication systems, video and audio applications. A typical SoC design contains multiple individual building blocks or cores, which can be processors, memories, input and output interface (IO), analogue, mixed- signal and radio- frequency (RF) circuits, etc [ITR09]. However, the test cost of the individual parts is very different from each other. The test cost per mm^2 of mixed- signal blocks is at least 10 times higher than digital blocks [Ara10]. Due to the recent innovative test technology, the test cost of digital blocks has been dramatically reduced. However, the analogue and mixed- signal test technology develop relatively slow resulting in a growing contribution of mixed-signal test cost to the overall SoC test cost. In a SoC, the analogue, mixed- signal and RF dominate the production test cost, which can be up to 70% of the overall test costs [Ste11]. It is obvious that industry requires the innovations of mixed- signal test technology to test them efficiently.

1.2 Mixed-signal testing

Mixed-signal circuits are widely used in our daily life nowadays [Vri10]. As the technology is developing, people design mixed-signal circuits with increased performance. Apart from the design, how to test mixed-signal circuits efficiently and accurately is also very important as well. It will directly determine whether the devices can be delivered to the customers in time with a good quality. However, this is not an easy task. In this section, the basic knowledge of mixed-signal testing is introduced and its bottlenecks are also explained.

1.2.1 Mixed-signal testing in a production environment

Mixed-signal circuits can be defined as circuits including both analogue and digital components [Bur00]. Typical mixed-signal circuits are analogue-to-digital converters (ADC) and digital-to-analogue converters (DAC); they are considered as the interfaces between the analogue and the digital world. Another typical mixed-signal circuit is the phase-locked loop (PLL), which is used to generate high-frequency clock signals or clock signals with a certain phase shift from the reference clock [Sai11]. An RF front-end is also a very widely used mixed- signal circuit as they are crucial part of the communication systems. It is used to convert the received RF signal to the desired original signal to modulate the original signal to an RF signal for transmission. Mixed- signal circuits are usually integrated into all kinds of applications, like mobile phones, motor controllers, audio and video products.

The fabrication process of the integrated circuit (IC) is very complex and unfortunately imperfect. It introduces all kinds of faults in the fabricated circuits. As a result, production testing is required after the fabrication of the mixed-signal circuits. The main purpose of production testing is to guarantee the specification and the function of the application of the customer. It can be considered as a process to guarantee the quality of the IC products, which plays a very important role in the IC industry. The production testing usually encompasses three steps [Bur00]:

1. **Test of silicon wafers**. After the silicon wafers of the circuits have been fabricated, wafer testing must be carried out to discard the bad dies by using automatic test equipment (ATE). This testing is only used to decide which silicon dies pass or fail.
2. **Packaging.** The die which passes the wafer testing will be packaged
3. **Final testing.** The final testing is carried out on the packaged devices to guarantee the performance of the devices after packaging. Another ATE different from the one used for wafer testing will be exploited for the final testing.

The production testing of mixed-signal circuits should have the following features [Phl03]:

- Its main purpose is to guarantee that only good devices are shipped to the customer.
- It has to extract the information for characterization, yield monitoring and analysis of the fabricated chips.
- A large number of Devices-under-Test (DUT).
- It should be optimized to achieve sufficient accuracy but minimum test time per product. A typical test time for a data converter can be from 10 ms to 100 ms depending on its resolution.
- The equipment used are ATEs especially developed for mass–volume production testing.

1.2.2 Mixed-signal test equipment

The ATEs used for mixed- signal testing mainly contain a test head, a workstation and the main cabinet [Bur00]. A photo of a mixed- signal test system from Advantest is shown in Figure 1.1. The computer workstation is the interface between the ATE and the test engineer.

The engineers can control the ATE by software in the workstation and the test results can also be stored and shown on it. The main cabinet consists of power supplies and measurement instruments. The test head contains the most sensitive measurement units. For example, if a very high- speed digital signal is applied to the DUT, the digital driver should be put on the test head as close as possible to the DUT. An ATE for mixed- signal testing can cost 2 million dollars or even more [Bur00].

Figure 1.1: Photo of the T7723 mixed- signal test system from Advantest

A device interface board (DIB) is designed as the electrical interface between the ATE and the DUT. It has the socket connecting the DUT to the ATE. It also contains the specific circuits for the DUT. Normally the circuits are pull- up resistors, capacitor loads or buffers. Complex circuits are not preferred on the DIBs, like data converters large capacitors or filters [Pr106]. First, it will increase the cost of the DIBs. Second, the complexity of the DIBs will increase as well. The DIB itself has to be tested first before production testing. If there are some complex circuits on the DIB, the test time of the DIB will increase.

For wafer testing, wafer probers are required. They are robotic machines to manipulate wafers tested by the ATE. It moves the wafers accurately in order to connect the contact pads on the wafers to the tips of the probes. For package testing, handlers are used to manipulate packaged DUTs in a similar way as the wafer probers. Summarizing, the wafer probers and the handlers make a temporary connection between the DUTs and the ATE.

Just from the hardware requirements of the mixed- signal production testing, one can understand that it is an expensive business that adds to the cost of a chip.

1.2.3 Mixed-signal testing challenges

Before production testing is carried out, a lot of time has to be spent on preparation work for testing, like defining the test plan, designing the test hardware, writing test code. Because they require a lot of time, they can directly influence the time to market of the products. [Che05]

The real measurement environment is not as ideal as a simulation environment. Mixed-signal circuits are very sensitive and hence a lot of problems can cause inaccurate results. We mention, among many others, electromagnetic interference, improperly calibrated instruments, and an incorrect test environment.

One of the most important issues in production testing is the test cost. The test equipment and the test time are two major factors influencing the test cost. As mixed-signal circuits contain both digital and analogue components, the mixed-signal testing usually requires high quality analogue signal sources, high-resolution converters, or a high quality clock signal. Compared with the ATE for testing digital circuits, the one for testing mixed-signal circuits is much more expensive.

Nowadays, the trend in ICs is to reduce the size of transistors and hence increase the number of transistors, in order to enable the systems to have more functionality but with smaller size. For digital circuits, this trend is very fast. It results in significant changes of digital circuit testing in recent decades. There are few functional tests and mainly structural tests. However, for mixed-signal circuits, this trend is relatively slow. Mixed-signal testing still uses functional and parametric testing, which is very complex and time-consuming. Main reason is the absence of a general fault model.

1.3 Mixed–signal built-in self test

Built-In Self Test (BIST) is the approach in which the device-under-test (DUT) can test itself without elaborate ATE support [Bur00]. Normally, it requires additional circuits on-chip in order to generate the test input stimuli or extract the test results.

Nowadays, multi-site testing is a very popular method to reduce the production test time. In multi-site testing, multiple chips can be tested in parallel on the same test head. In this way, it reduces the overall test time. Nevertheless it requires additional test instruments, which can

be very expensive. For example, a high- resolution arbitrary waveform generator can cost more than 30 000 dollars. As the BIST technology relaxes the requirement of the ATEs, the multi-site testing can be implemented much easier and cheaper [Hue04]. Unfortunately, the implementation of BIST technology in mixed-signal testing is relatively rare. The main reason is that there is always a trade off between the test accuracy and the overhead of silicon area. In order to guarantee the accuracy of the signal generation and the measurements on-chip, it requires relatively complex additional circuits for BIST. In this case, it will result in an overhead of silicon area. The other reason is that as the mixed-signal circuits are very sensitive, the additional circuits for BIST could possibly influence the performance of the circuits under test. In industry, Mentor Graphic is the major company providing general BIST solutions. In 2010, it has 98% of the BIST market share. In recent years, ATEEDA are also investigating the EDA tools for analogue and mixed- signal BIST. It announced the world's first push button analogue BIST tool in 2009.

1.4 Motivation

The ADC is one of the most typical and widely used mixed-signal circuits. Therefore, it is selected as the target device of our research work on mixed- signal testing. In recent years, many ADCs are integrated into platform-based designs, which are widely applied in video, audio, and high-speed communication systems. The architecture of the platform normally contains standard blocks such as memories and digital processors, RF and analogue front-ends. Testing such a system is a very complex task. The related test cost is a major part of overall chip costs [Ara10]. Due to the nature of mixed-signal testing discussed in section 1.1.3, the test cost of ADCs has a relatively high percentage of the total test cost of the chips. A solution to cut down the test costs is to reuse the on-chip resources to perform the BIST of ADCs. In this case, the requirements of the test equipment can be relaxed. Moreover, multi-site testing can be implemented in a much cheaper way. More ADCs can be tested in parallel without expensive additional test equipment.

When investigating the test solutions of the ADC, there are also some constraints on the circuits for test purposes. First, as mentioned above, too many or complex circuits on the DIBs are not preferred. For example, if a high-resolution DAC is used as the signal generator, this is not the preferred approach (by NXP Semiconductors). Obviously, more circuits will increase the cost of the DIBs. Moreover, the DIBs are required to be tested before the production testing can start. As there are complex circuits on them, it means more time has to

be spent on DIB testing. If they are broken, more cost has to spend for replacement. Second, the additional circuits on the DUT for test purposes are also not preferred to be too large and should not affect the ADC circuits themselves. As the ADCs are complex and sensitive, the additional circuits must avoid affecting the performance of the ADCs. If the additional circuits for ADC test purposes are added, the silicon area of the whole chip will increase. In production testing, the additional circuits also have to be tested. If they are too large or complex, the silicon area and test time of the chips will increase as well. As a result, the benefits of the test circuits will become much less.

1.5 Outline of this thesis

This thesis is focused on investigating potential BIST test methods for ADCs, one of the most common mixed-signal circuits, using an embedded digital processor. The body of the thesis is organized as follows:

In *chapter 2*, typical ADC architectures are introduced, like sigma-delta, successive approximation, flash and pipelined designs. The conventional test method applied to ADCs is also explained, which mainly includes static and dynamic testing. After that, the bottleneck of the conventional ADC production testing is discussed. At the end of this chapter, we propose the basic structure of ADC testing using an embedded digital processor.

The required pulse waves with different forms are exploited to test the dynamic parameters of the ADCs in *chapter 3*. Instead of using a sine wave in the conventional test method, a pulse wave is investigated as the test stimulus. Two methods are presented: one is tuning the duty cycles; the other is increasing the number of the voltage levels of the pulse wave. Both simulations and measurements have been carried out on the ADCs to validate the proposed methods.

Chapter 4 proposes a pre-test concept to filter out faulty devices before carrying out complex conventional testing. An adaptive pulse wave is applied as test stimulus. Three different algorithms are proposed to realize the pre-test. The principle of the algorithm is evaluating the performance of a DUT by comparing the output between the golden devices and the DUTs in amplitude, angle or frequency. The methods are validated via simulations and measurements on a 6-bit flash ADC and a 12-bit pipelined ADC.

In *Chapter 5*, machine-learning-based testing for ADCs is presented. It can predict the specifications of ADCs by using low-cost signature testing. For the DUTs, only simple

signature testing is required. By substituting the signature results of the DUTs into the mapping function, the prediction results of the dynamic specifications of the DUTs can be calculated. A 12-bit pipelined ADC is used to validate the method in both simulations and measurements.

Chapter 6 summarizes the research results of the project versus the goals. It also gives recommendation for future research work to apply testing of ADCs by using embedded processors.

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Chapter 2

Analogue-to-Digital Converter Testing

2.1 Abstract

In this chapter, conventional ADC production testing is introduced and discussed. At first, typical ADC architectures and their state-of-art are introduced. It includes the pipelined and flash ADCs. After that, the key parameters in ADC production testing are explained. They are classified into static and dynamic parameters. The bottlenecks of testing key parameters are also analyzed. Then the state-of-art of both static and dynamic testing is investigated. Finally, we propose a potential BIST structure of reusing on-chip hardware resources based on the current platform design approaches.

2.2 Introduction

ADCs are one of the most widely used mixed-signal circuits, which are used to convert an analogue signal into a digital signal. It is an important interface between the analogue and digital world. In the electronic world, digitalization is the main trend. However, the real

world is analogue. As a result, ADCs are increasingly in demand. There are several different architectures of ADCs. Table 2.1 briefly summarizes the typical characteristics of several typical ADC architectures [Mar10]. Depending on the requirement of the application, the proper type of ADC has to be selected. In this section, several typical ADC architectures will be introduced.

Table 2.1: Typical characteristics of different ADC architectures [Mar10]

Type of analog-to-digital converter	Clock cycles for N bit conversion	Specification BW = Bandwidth
Full-flash converter	1	very fast, BW = 1 GHz, $N <$ 6–8, power hungry
Folding converter	1	$N < 8, 9$
Pipeline	N	$N <$ 12–14, fast, BW = 10–200 MHz, efficient, latency of $>N$ clock cycles
Successive approximation	N	Compact, BW = 2–5 MHz, N <12, low power
Sigma-delta	20–50	N up to 24, BW = 100 Hz – 5 MHz
Dual-slope	2^N	N = 14–20, BW = 10 kHz

2.2.1 Flash analogue-to-converters

The flash ADC is a very basic architecture of ADCs. Except using it as a stand-alone ADC, it is also often applied in other more complex ADC architectures as sub-ADCs. In this thesis, one of the target devices is a flash ADC, whose architecture is shown in Figure 2.1. An analogue input is applied to one side of a comparator circuit and the other side is connected to

the proper level of reference from the lowest level to full scale. The threshold levels are usually generated by resistively dividing one or more references into a series of equally spaced voltages, which are applied to one input of each comparator. The total number of comparators required is 2^{n-1}, where n is the resolution of the ADC. If the resolution is very high, the large number of comparators causes various detrimental effects:

- Large die size which implies high cost, large device count leading to low yield.
- Complicated clock and signal distribution with significant capacitive loading.
- Large input capacitance requiring high power dissipation in the S/H driving the A/D converter and degrading dynamic linearity.
- High power-supply noise due to a large digital switching current.
- Significant errors in threshold voltages caused by comparator input bias current flowing through the resistive reference ladder.

These factors make implementation of flash converters exceeding 8 bits very difficult, especially if low power dissipation is required. An S/H amplifier for sampling of the input signal is not a necessary component for the flash A/D converter. However, since the CMOS high-speed comparator usually contains a differential amplifier at its input, the insertion of an S/H amplifier in front of each comparator can help avoiding:

- Improper signal racing among the differential amplifiers of the parallel connected high-speed comparators
- Reduce the input impedances.
- Increase the analogue bandwidth of the whole conversion system.

Basically, the performance of a low-resolution flash A/D converter is limited primarily by the accuracy of the comparators and secondarily by the accuracy of the reference. To ease the problem of the large input capacitance, the difference between the analogue input and each reference voltage can be quantized at the output of each pre-amplifier, which is possible because of the finite gain of the pre-amplifier (non-zero linear input range). This indicates that interpolating between the outputs of pre-amplifiers can increase the equivalent resolution of a flash stage [Ste93]. The gain in the pre-amplifiers reduces the required accuracy and thereby the power consumption of the comparators.

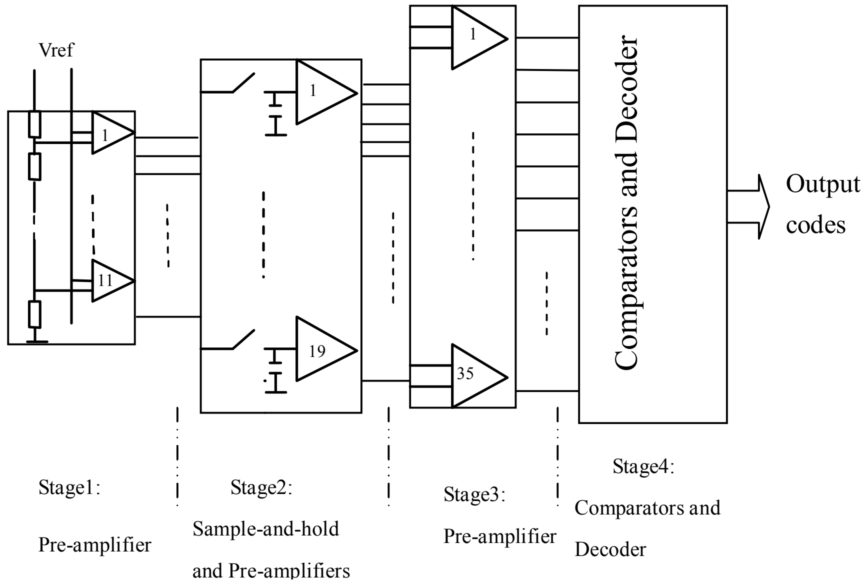

Figure 2.1: The block diagram of a 6-bit flash ADC [Bur00]

Recently, some research works have been carried out on the design of the flash ADCs. In [Cha11], a 12 GS/s 5-bit time-interleaved flash ADC is presented. A calibration technique for time skew is exploited to improve the dynamic performance. The power consumption is reduced by applying comparators of small-sized transistors. In order to reduce the offset of the comparators, trimming circuits are exploited for each comparator respectively. Finally, the design has been fabricated in 65 nm CMOS and validated by measurements. A 4- bit 700 MS/s flash ADC is reported in [Tor11]. It is designed in a 0.18 µm CMOS process. A comparator with built-in reference voltages is used in this work. It eliminates the need of the resistor ladder and its power consumption. A calibration technique is also applied to reduce the noise of the comparator. In this case, the power consumption can be further improved.

2.2.2 Pipelined analogue-to-converters

The pipelined ADC is a very popular choice in high-speed and high-resolution applications [Mos01]. The key advantages of a pipelined ADC are the high conversion rate, high resolution, good dynamic performance and low power consumption. The architecture of a 12-bit ADC is shown in Figure 2.2 [Gee06]. This is also one of the target devices in this

thesis. It consists of ten stages: the first two stages are 2.5 bits composing of a multiplying DAC (MDAC) and a flash ADC with six comparators. There are 6 different levels of the reference voltages of the 6 comparators, which means the input range of the ADC is divided into 7 regions. Each of the seven stages in the middle is 1 bit which has an identical architecture as the first two stages. The last stage is 1.5 bits which is a flash ADC. The first stage only accomplishes a coarse conversion. In the second stage, the differential signal between the original input and the first stage output is further converted to a higher resolution. In this way, the input signal is converted stage by stage. At the end, the results of every stage are combined to achieve a high-resolution output. The basic architecture of each stage is identical, which is denoted with the dashed box in Figure 2.2. Its major parts are a residue amplifier, an analogue adder, a 1.5-bit ADC and a 1.5-bit DAC. Usually the ADC in the sub-stage is implemented by a flash ADC. As the resolution of a sub-stage is very low, only a few comparators are required to build up the flash ADC.

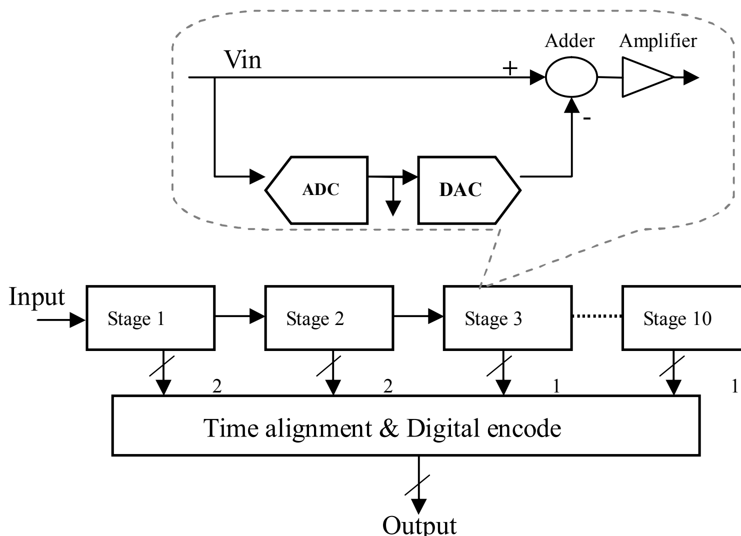

Figure 2.2: The block diagram of a 12-bit pipelined ADC

The MDAC is a very critical circuit in a pipelined ADC. The amplifier, adder and DAC blocks in Figure 2.2 are all implemented by a multiplying DAC (MDAC) [Pla94]. The typical MDAC is composed of a switched-capacitor circuit. Figure 2.3 shows an example of a 1.5 bit MDAC [Car06]. At the first clock phase Φ1, the signal is sampled and stored (hold) on the capacitors C_F and C_S. At the second clock phase Φ2, C_F is switched to the feedback path of

the amplifier and C_S is connected to the reference voltage. At the end, the signal is amplified and subtracted by the reference voltage. The performance of the MDACs will affect the speed limit and accuracy of the pipelined ADCs directly. In the MDAC, the major factor which limits the accuracy is the mismatch of the capacitors.

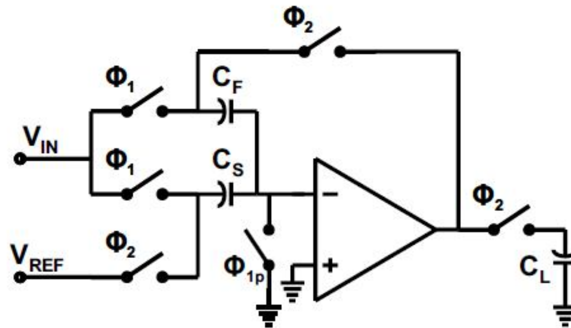

Figure 2.3: The block diagram of a 1.5-bit MADC [Car06]

Now, some recent designs of pipelined ADCs are presented. A 10-bit, 100 MS/s pipelined ADC is reported in [Kim11]. It exploits an input-swapped opamp-sharing technique and a voltage-to-current converter with automatic error correction. In this case, it can achieve low power consumption and a small area. It is fabricated in a 0.18 μm CMOS process and validated by measurements. In [Wan09], a 12-bit 20 MS/s pipelined ADC is presented. In order to reduce the power consumption, the sample-and-hold circuit is removed. As alternative, a digital timing compensation method is applied. The ADC is fabricated in 0.35μm CMOS process. The measurement results show that it can achieve low power consumption.

2.3 Key testing parameters of ADCs

The key parameters of ADC testing can be classified into two types of testing: one is static parameters and the other is dynamic parameters. The static parameters evaluate the transfer curve of the ADC under test with the ideal one. It includes gain, offset, the differential non-linearity (INL) and the integral non-linearity (INL).

The dynamic parameters evaluate the dynamic performance of the ADC, including total

harmonic distortion (THD), signal-to-noise ratio (SNR), signal-to-noise-and-distortion (SINAD) and spurious free dynamic range (SFDR).

In this section, the definition of both static and dynamic parameters of ADCs will be introduced first. Then, the conventional test methods in production testing are explained. Moreover, the state- of- art of the ADC test methods are also investigated. Finally, the main bottle- neck in present ADC production testing is analyzed.

2.3.1 Static parameters

The ideal transfer function of a 3-bit ADC is shown in Figure 2.4. The x-axis denotes the continuous analogue input voltage while the y-axis denotes the discrete digital output. As the input voltage reaches a certain threshold level, the output code changes; one can observe from the figure that the Least Significant Bit (LSB) is defined as:

$$LSB = \frac{FS}{2^n} \tag{2.1}$$

, where *FS* is the full scale of the input voltage and *n* is the resolution of an ADC. The *LSB* is used as the unit to represent linearity errors of ADCs. In Figure 2.4, one can observe that each code corresponds to a certain range of the input voltage levels.

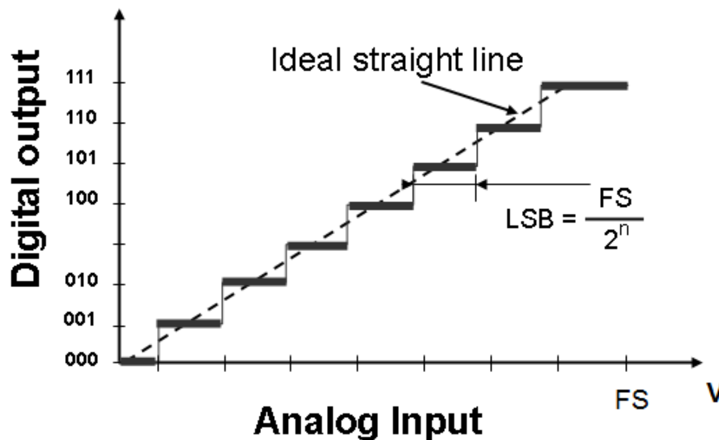

Figure 2.4: Ideal transfer function of a 3-bit ADC

- **The Differential Non Linearity (DNL)**

DNL is the difference between a step in LSB of the ADC transfer function and the ideal

value of 1 LSB [Bur00]. The DNL of an ADC less than 1 LSB guarantees a monotonic transfer function without missing code. It is defined as [Bur00]:

$$DNL(i) = \frac{V_{i+1} - V_i}{V_{LSB\ ideal}} - 1 \quad LSB, \quad i = 1, 2, \ldots 2^n - 2 \tag{2.2}$$

, where V_i represents the *voltage value* corresponding to the digital code *i* and $V_{LSB\ ideal}$ is the ideal *voltage difference* between two adjacent digital codes. The DNL is 0 LSB in an ideal ADC transfer function, as each step equals to 1 LSB. The overall DNL of an ADC is specified as the maximum absolute value of the numbers found from equation (2.2).

- **Integral Non Linearity (INL)**

INL is defined as the deviation of the transfer function from an ideal straight line [Bur00]. The ideal straight line can be the best-fit line or the end-point line. The best-fit line is the straight line closest to the actual transfer function of the ADC, while the end-point line is the straight line drawn through end points of the ADC's transfer function. It can be calculated as:

$$INL(i) = \left| \frac{V_i - V_0}{V_{LSB ideal}} \right| - i\ LSB,\ where\ i = 1, 2, \cdots 2^n - 2 \tag{2.3}$$

, where V_0 is the input voltage of the ADC when the output code is 0. The overall INL of an ADC is defined as the maximum absolute value of the numbers in equation (2.3).

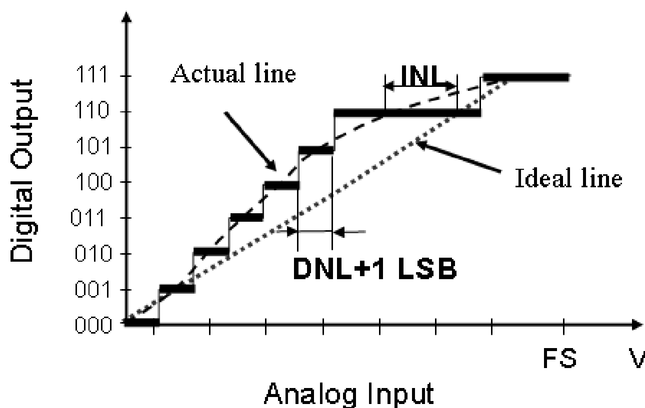

Figure 2.5: The INL and DNL of a 3-bit ADC

- **Gain error**

Gain is the slope of the best-fit straight line of the transfer function of the ADC. The gain error is the ratio between the actual slope and the ideal one (see Figure 2.6). It can be defined as:

$$Gain\ error = \frac{Gain_{real} - Gain_{ideal}}{Gain_{ideal}} * 100\% \tag{2.4}$$

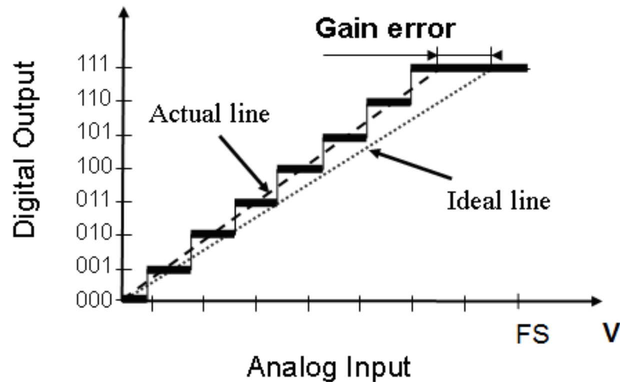

Figure 2.6: The gain error of a 3-bit ADC

- **Offset error**

Offset is the intersection point of the best fit straight line of the transfer function of the ADC with the x-axis. An offset error is the deviation of the actual offset voltage from the ideal one.

$$Offset\ error = Offset_{real} - Offset_{ideal} \quad LSB \tag{2.5}$$

Table 2.2: Static characteristics of the 12-bit pipelined ADC [NXP09]

Parameters	Conditions	Min	Typical	Max	Unit
Static characteristics @ Fs = 50MS/s					
INL	Fin=1.8MHz	-	+/- 1.0	+/- 2.5	LSB
DNL	Fin=1.8MHz	-	+/-0.5	+/-1.0	LSB
Static characteristics @ Fs = 80MS/s					
INL	Fin=1.8MHz	-	+/- 1.5	+/- 3.0	LSB
DNL	Fin=1.8MHz	-	+/-0.5	+/-1.0	LSB

As an example, a part of the static characteristics of the 12-bit pipelined ADC in Figure 2.2 are shown in Table 2.2 [NXP09], where Fs and Fin are the sampling frequency and input signal frequency respectively. However, the gain error and offset error are not included in the data sheet of this 12-bit pipelined ADC.

2.3.2 Conventional ADC testing of static parameters

The conventional test setup of ADC production testing is shown in Figure 2.7. The waveform generator is normally an arbitrary waveform generator (AWG). The digital output data is stored in the memory and then transferred to the DSP to calculate the test results, like INL, DNL. All the clocks should be synchronized in order to apply coherent sampling [Bur00]. Sometimes, if the purity of the spectrum of the input signal is insufficient, a filter must be added between the waveform generator and the ADC.

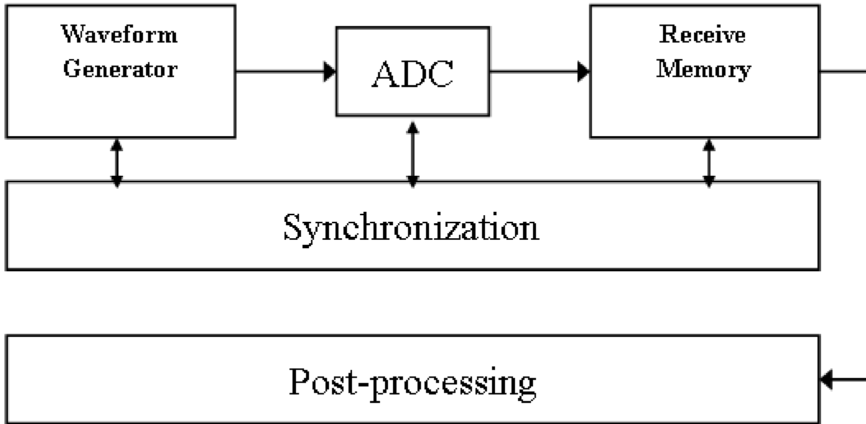

Figure 2.7: Test setup of an ADC conventional test

1) Nonlinearity testing with a ramp signal

Nowadays, a histogram method is usually applied to test the static parameters of the ADCs [Bur00]. It requires that the voltage distribution of the input test stimulus must be known. For example, a linear ramp signal has an even distribution of the voltage levels. Usually, a ramp signal or a sine wave signal is selected as the test input signal. As the ADCs are excited by the input signals, the output samples of the ADCs are collected at a constant sampling rate. After that, the DSP will calculate the results of the histogram method. It will show how many times a code appears at its output with the corresponding input analogue signal. For an ideal ADC, each code should be hit the same number of times with a linear ramp input signal. If one assumes that *H(i)* is the number of hits of the code *i* and *n* is the resolution of the ADC under test, then the average hits per code can be calculated as [Bur00]:

$$H_{average} = \frac{\sum_{i=1}^{2^n-2} H(i)}{2^n - 2}, \quad i = 1,2,\ldots 2^n - 2 \tag{2.6}$$

Then the code width of each code in LSB can be calculated as:

$$C(i) = \frac{H(i)}{H_{average}} \quad LSB, \quad i = 1,2,\ldots 2^n - 2 \tag{2.7}$$

The DNL can be calculated as:

$$DNL(i) = C(i+1) - 1 \quad LSB, \quad i = 1, 2, \ldots 2^n - 2$$

(2.8)

At last, the overall DNL can be calculated as:

$$DNL = Max\left|C(i+1) - 1\right| \quad LSB, \quad i = 1, 2, \ldots 2^n - 2$$

(2.9)

The overall INL can be calculated as [Bur00]:

$$INL = Max\left|\sum_{i=1}^{2^n-2} DNL(i)\right| \quad LSB, \quad i = 1, 2, \ldots 2^n - 2 \qquad (2.10)$$

For more accuracy and better repeatability of the measurement results, each code should be hit as many times as possible. However, a very long test time in production test can not be accepted. In practice, 16 or 32 hits per code are typically used.

2) Nonlinearity testing with a sine wave signal

A sine wave is also commonly used as input stimulus for testing the nonlinearity. In order to hit all codes of the ADCs, the amplitude of the sine wave input signal is usually larger than the input range of the ADCs. Compared with a ramp signal, a sine wave has an uneven distribution of the voltages. It has more samples on the upper or lower peak than the center. A sine wave input and its corresponding histogram plot is shown in Figure 2.8. As result, the code hits of each voltage level are different even for an ideal ADC. However, the distribution of the voltage levels of a sine wave is known. In this case, the compensation can be carried out for the uneven distribution.

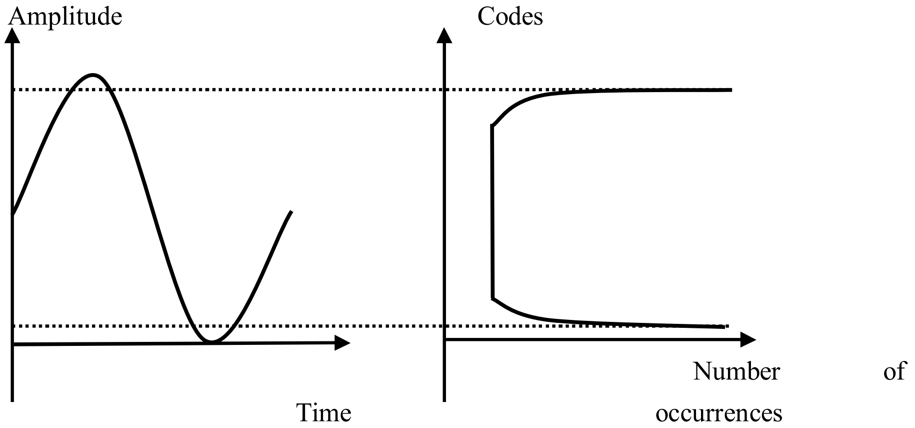

Figure 2.8: Sine wave and its corresponding histogram [Bur00]

If one assumes *H1* and *H2* to be the number of code hits of the upper and lower peak, *Ns* is the total number of samples and *n* is the resolution of the ADC, then the amplitude and offset of the sine wave in *LSB* can be calculated as [Bur00]:

$$Offset = \frac{\cos(\pi \frac{H2}{Ns}) - \cos(\pi \frac{H1}{Ns})}{\cos(\pi \frac{H2}{Ns}) + \cos(\pi \frac{H1}{Ns})} * (2^{n-1} - 1) \quad LSB \tag{2.11}$$

$$Amplitude = \frac{2^{n-1} - 1 - Offset}{\cos(\pi \frac{H1}{Ns})} \quad LSB \tag{2.12}$$

After that, the ideal histogram of each code of the ADC, which is obtained by the ideal ADC and the ideal measurement setup, can be calculated as:

$$H_{ideal}(i) = \frac{Ns}{\pi}\left[\arcsin\left(\frac{i + 1 - 2^{n-1} - Offset}{Amplitude}\right) - \arcsin\left(\frac{i - 2^{n-1} - Offset}{Amplitude}\right)\right] \tag{2.13}$$

After H_{ideal} is obtained, the *DNL* and *INL* can be calculated in a similar way as shown in the equations (2.7), (2.8), (2.9) and (2.10). Instead of using $H_{average}$, H_{ideal} is used in equation (2.7).

2.3.3 Dynamic parameters

The main dynamic parameters in ADC production testing include THD, SINAD, SNR and SFDR. In this section, the basic definition of these parameters is explained.

Total Harmonic Distortion (THD): The THD is the ratio of the power of the harmonics to the power of the fundamental frequency. It can be defined as [Phl03]:

$$THD = 10\log\left(\frac{P_{harmonics}}{P_{signal}}\right) \quad dB \tag{2.14}$$

Where:

$$P_{harmonics} = a_2^2 + a_3^2 ... + a_k^2$$

$$P_{signal} = a_1^2$$

$P_{harmonics}$ denotes the power of the harmonics; P_{signal} denotes the power of the output signal; a_1 is the magnitude of the fundamental; a_k is the magnitude of the kth harmonic. The number of harmonics in the calculation of *THD* depends on the requirement of the application. Normally, using five harmonics for the calculation of $P_{harmonics}$ is sufficient [Kes08].

Signal-to-noise ratio (SNR): The SNR is defined as the ratio of the output signal power to the noise power, excluding the harmonic power [Kes08]. The bandwidth of the noise for calculation is $f_s/2$, where f_s is the sampling frequency of the ADCs. It is therefore defined as [Phl03]:

$$SNR = 10\log\left(\frac{P_{signal}}{P_{noise}}\right) \quad dB \tag{2.15}$$

P_{noise} is the power of noise.

Signal-to-noise-and-distortion (SINAD): The SINAD is the ratio of the output signal power to the noise plus the distortion power. It has been defined as [Phl03]:

$$SINAD = 10\log\left(\frac{P_{signal}}{P_{noise+distortion}}\right) \quad dB \tag{2.16}$$

Spurious Free Dynamic Range (SFDR): The SFDR specifies the ratio of the amplitude of the fundamental and the amplitude of the peak spurious content in the frequency band of interest [Kes08]. The peak spurious can be the harmonics or the noise in the band. In general, the frequency band of interest ranges from *DC* to $f_s/2$, where f_s is the sampling frequency of the ADC. The spurious content includes all types of distortion, regardless of their origin. It can be calculated as [Phl03]:

$$SFDR = 20\log\left(\frac{a_1}{\max(s)}\right) \quad dB \tag{2.17}$$

, where a_1 is the amplitude of the output fundamental and $max(s)$ is the maximum amplitude of all the spurious components.

Effective Number of Bits (ENOB): The ENOB represents the ideal resolution of an ADC with the SINAD measured on the real ADC. It can be obtained as [Phl03]:

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad dB \tag{2.18}$$

As an example, the dynamic specification of the 12-bit pipelined ADC in Figure 2.2 is shown in Table 2.3.

Table 2.3: Dynamic characteristics of the 12-bit pipelined ADC [NXP09]

Parameters	Conditions	Min	Typical	Max	Unit
Dynamic characteristics @ Fs = 50MS/s					
ENOB	Fin=1.8MHz	10	10.3	-	LSB
SNR	Fin=1.8MHz	62	64	-	dB
THD	Fin=1.8MHz	-	-75	-65	dB
SFDR	Fin=1.8MHz	65	75	-	dB
Dynamic characteristics @ Fs = 80MS/s					
ENOB	Fin=1.8MHz	9.8	10.3	-	LSB
SNR	Fin=1.8MHz	62	64	-	dB
THD	Fin=1.8MHz	-	-70	-65	dB
SFDR	Fin=1.8MHz	65	75	-	dB

2.3.4 Conventional ADC testing of dynamic parameters

All dynamic parameters of ADCs can be obtained from the analysis in the frequency domain. At present, the Fast Fourier transform (FFT) computation is normally carried out in order to obtain the dynamic parameters. The FFT converts a signal in the time domain to its

representation in the frequency domain. For the input signal, a sine wave is required. Normally, coherent sampling is applied for FFT analysis. If one defines f_{in} the frequency of the input sine wave, f_s is the sampling frequency of the ADC, M is the number of periods of the input signal and N the number of samples, then they should satisfy the following conditions:

$$\frac{f_{in}}{f_s} = \frac{M}{N}, M \text{ and } N \text{ are coprime} \tag{2.19}$$

If M and N cannot satisfy the condition, it is called non-coherent sampling. The non-coherent samples cannot be used to form a continuous signal through a looping process. In this case, the output data samples have to be analyzed by a technique called *windowing*. However, it is not preferred in production testing [Bur00].

2.3.5 Bottlenecks in ADC production testing

ADC production testing is a specification-based testing approach. As introduced in the previous sections, both the static and dynamic parameters have to be tested, which can not be obtained within a single test. In static ADC testing, the accuracy and repeatability are directly related to the resolution of the input signal generator and the number of samples per code. Therefore, the resolution of the input signal has to be better than 0.1 LSB and the number of samples is averaged 10 samples per code in general [Bur00].

In dynamic testing, as a rule of thumb, the noise level of the input signal should be at least 10 dB lower than the ideal value of SINAD of the ADC under test [Phl03]. Because of the developments of the digital circuits nowadays, the resolution and speed of ADCs are increasing increasingly high. As a result, the quality of the input signal has to be higher, which makes the signal generator more expensive. Moreover, as more samples are needed in order to obtain accurate test results, longer test times and a higher computation power of the processors will be required.

As introduced in Chapter 1, multi-site testing is an efficient way to reduce the test time. However, multi-site test is difficult to implement for ADC testing. The increasing number of sites will require extra test instruments. For example, the input signal generator, which is normally expensive. Therefore, the number of sites for mixed-signal testing is usually up to 8. Summarizing, at moment the major bottlenecks in ADC production testing are: 1) the expensive signal generator, 2) the required test time and 3) required computational power.

2.3.6 State- of- the art of static parameters ADC testing

As the resolution and speed of the ADCs become higher, the conventional histogram-based static testing of ADCs will require more test time and a higher quality of the input signal. As a result, much research has been carried out to investigate new test methods for static parameters.

The method in [Gin11] proposes a novel solution for INL measurements instead of using the histogram method. It is realized by simple digital computational circuits. It overcomes the complexity of the histogram- based method. As result, it can be useful for BIST of ADC and simple digital ATE- based ADC static testing. The method is validated on an 11-bit pipelined ADC and a 14- bit pipelined ADC. The results show that the accuracy is in the same order of magnitude as the standard histogram method.

[Kor11] proposes a method for static testing of DAC- ADC pairs, which only requires a low- quality input test stimulus and a small memory. A DAC generates the test input signal of the ADC. An offset voltage is added to the output of the DAC. It is used for distinguishing the nonlinearity errors between the ADC and the DAC. The test results are split into small parts. In this case, the full histogram can be transformed into small ones. As a result, the memory size can be reduced. The test method is validated by the measurement of a 12- bit ADC and a 12- bit DAC.

A method using a nonlinear ramp signal for ADC static testing is proposed in [Vor10]. The method is based on the concept that a nonlinear ramp signal can be considered as a combination of a number of short segments. The assumption is that some of the segments are much more linear than the whole ramp signal. The most linear part of the nonlinear ramp signal is applied to the ADC as the test stimulus by optimizing the amplitude of the ramp signal. The measurement on an 8- bit ADC and a 10- bit ADC have been used to validate the proposed method. As result, the requirement of the linearity of the ramp stimulus can be relaxed.

In [Nis09], a new test method for INL is proposed. Only a dc voltage source with the white Gaussian noise is applied as the test input signal. The method repeats the measurements of the DUT. After that, the transition level of each code of the ADC can be estimated from statistic analysis. Compared with the conventional test method, it is much faster, as it requires fewer samples. The requirement of the resolution of the input signal is relaxed, which does not have to be higher than the DUT. The method is validated by both

simulation and measurement results.

[Wen08] proposes a BIST structure for testing ADC static parameters, including gain error, offset error, *INL* and *DNL*. The BIST circuitry is composed of a control circuit, a differential integrator, a counter and a test-response analyzer. The test input ramp stimulus is generated by the control unit and the differential unit. The system clock triggers both the counter and the control unit. In this case, the input ramp signal of the ADC and the counter are synchronized. The test response analyzer can take the code of the counter as the reference for analyzing the output of the ADC. The method is validated on 12- bit ADC.

As a conclusion, the trend of the static testing of ADCs is:

1) Relax the requirement of the input signal as the work in [Kor11], [Vor10] and [Nis09].

2) In stead of the histogram method, use another analysis method to relax the computational power and time as the work in [Gin11] and [Nis09].

3) Use a BIST structure as the work in [Wen08].

2.3.7 State- of- the art of dynamic parameter ADC testing

Nowadays, several researchers are investigating ADC dynamic testing. Their purpose is to reduce the test time and the cost of the signal generator.

In [Dua10], the dynamic parameters are estimated from the INL of the ADC. In this case, the dynamic testing can be combined with static testing. The total test time can therefore be reduced. This method does not require an additional sinusoidal source. The INL is used to compute the power of the harmonics of the ADC. The THD and the SFDR are estimated. The computational requirement is very small compared to the spectral analysis. A measurement of a 16- bit SAR ADC was carried out to validate the method.

[Jia05] reports a test method for ADC dynamic testing using a segmented thermometer coded DAC. Dynamic element matching is an effective technique to achieve a good average performance if there is device mismatch. Based on this technique, a deterministic dynamic element matching scheme is applied to the DAC. In this case, the resolution of the DAC is not required to be as high as the ADC under test. In the simulation, a 12- bit DAC can be used as an 18- bit resolution DAC after applying the proposed method.

A novel test method in [Goy05] proposes a novel solution, based on

machine-learning-based test method, for testing high-speed ADC. One generates a high-frequency test input stimulus by mixing two low-frequency signals by mixers. Band-pass filters are applied to extract the desired signal, of which the frequency is the sum of the two low frequencies. In this case, the cost of signal generation is reduced. However, the quality of the extracted signal is not sufficient to obtain the dynamic parameters accurately. In this case, an unconventional test method is proposed. A prediction function is generated by the multivariate adaptive regression splines (MARS) [Fri91] and the data of training devices. Finally, by using the prediction function, the values of the dynamic parameters can be predicted from the signature results.

As a conclusion, the trend of the dynamic testing of ADCs is:

1) Reduce the test time by using unconventional test methods as the work in [Dua10].

2) Relax the requirement of the quality of the input signal as the work in [Koo09], [Koo11], [Jia05].

3) Use machine-learning-based method to estimate the dynamic parameters of ADCs as the work in [Goy05].

2.4 ADC testing using embedded processors

More and more mixed-signal system chips are becoming platform-based designs, which are widely used in audio, video or communication applications. These chips usually consist of a standardized architecture containing DSP, memories, RF and analog front-ends. Testing such mixed-signal systems is a complex task. The test time and related test cost is often a major part of the overall chip costs. In a mixed-signal system, ADCs are very commonly used devices. Due to the functional nature of ADC testing and the needs for more expensive test equipment, the test costs can be cut down by using the on-chip digital processors to perform the production testing.

The major bottlenecks in ADC production testing are expensive signal generators, the required test time and the computational power. As a DSP is very suitable for data processing, it can be used to process the digital output data of ADCs. It will relax the requirement of the computational power. The on-chip IPs can be reused as signal generator. For example, the memories, DSP or DACs all have the possibility to be used for signal generator. In this case, the cost of the signal generator can be reduced. As both data processing and signal generation

can be implemented by reusing the on-chip resources, a BIST structure of ADC has the potential to be developed on the platform. In this case, the digital processor can also be used to control the test flow.

In this thesis we will explore the possibilities of using embedded processors for ADC testing.

2.5 Conclusions

In this chapter, several typical architectures of ADCs have been introduced, like pipeline and flash converters. The major trend in ADC design is larger bandwidth, higher resolution and lower power consumption. The architecture of ADCs is selected in different applications according to their features and the specification of the applications.

The test parameters of ADCs include static and dynamic parameters. The static parameters are mainly INL, DNL, gain and offset, which evaluate the linearity of ADCs. They can be tested by a high quality ramp or a sine wave signal. The dynamic parameters are THD, SNR, SINAD, SFDR and ENOB, which evaluate the dynamic performance of ADCs. A sine wave is applied as the test stimulus and its input frequency, number of periods should satisfy the coherent sampling theory.

In conventional ADC production testing, the histogram method and FFT are the major techniques for static and dynamic testing respectively. As the resolution and speed of ADCs increases, more samples of output data and a higher quality of the input test signal are required. This of course directly affects the test time and cost. In this case, the bottleneck in ADC production testing is test time cost and the high requirement of the input test stimulus generator. Nowadays, a lot of research is being carried out to investigate how to overcome these bottle-necks. From the state-of-art of ADC test methods, one can see that BIST is one of the most promising techniques. The machine-learning-based test methods are also becoming more popular.

In the last section of this chapter, we propose to reuse the IPs on the platform for ADC testing, based on the fact that a large number of ADCs nowadays are integrated into an embedded platform design, which normally includes standard IPs like DSP and large memories. By reusing the hardware resources on-chip, the requirements of the ATE can be relaxed and multi-site test can be implemented much more easily for ADC production testing.

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Chapter 3

Determining ADC Dynamic Parameters via Adapted Pulse-Wave Input Stimulus

3.1 Abstract

As discussed in Chapter 2, the major bottleneck of ADC production testing is the generation of the input test signals. Because of the increase of speed and resolution of ADCs nowadays, the requirements of the quality of the input test stimuli also become increasingly higher; obviously this raises the cost of testing significantly. For this reason, finding a simple and inexpensive approach to generate input stimuli becomes crucial. The goal of our research is to reduce the cost of ADC testing by exploiting the wide availability of embedded digital processors. In this chapter we will present two test methods using pulse-wave as the test stimulus. The basic idea is emulating a sine-wave by using different forms of pulse-waves. The first method is using a sequence of pulse-waves with different duty-cycles as the test

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Parts of this chapter have been published in [She08] and [She09].

input signal. The second method is exploiting a pulse-wave with multi-steps. Compared with a high-quality analogue sine-wave, it is easier for a digital processor to generate a pulse-wave. In this case, the pulse-wave stimuli can save test time and cost.

3.2 Introduction

A high-quality analogue sine-wave or ramp is usually applied as test input stimulus in conventional ADC dynamic testing. After obtaining the digital output of the ADC under test, the output spectrum can be obtained by using FFT analysis. At the end, the dynamic parameters, like THD, SNR and SINAD can be calculated.

Nowadays usually one or more embedded digital processors coexist with ADCs in many systems, like communication, audio and video applications. In this case, a digital pulse-wave is relatively easy to generate as compared to a high-quality analogue sine-wave or ramp signal. In this chapter, a pulse-wave input stimulus is investigated to test an ADC and the output spectrum is exploited for analyzing the dynamic performance of the ADC.

Until now, several different types of signals have been proposed to decrease the cost or the requirements of accurate analogue signal generators for ADC testing.

White noise is used to test the INL and the DNL of an ADC based on spectrum analysis [Flo03]. With only white noise as the test stimulus, the output spectrum of the ADC is expected as flat as the one of the white noise. However, if there are faults in the ADC, some additional frequency components will appear at the output.

The work in [Vor09] exploits a high-frequency sine-wave modulated by a low-frequency ramp signal. By applying such a test signal, the simultaneous estimation of both dynamic and static parameters of ADCs can be obtained. The proposed test method is validated for an 8-bit ADC. It can reduce the test time and the number of signal sources as the dynamic and static tests are integrated into one test procedure.

The authors in [Rol06] propose a BIST test method for sigma-delta ADCs by applying a binary stream as the input signal. A sine-wave fitting algorithm is carried out to analyze the output data. Because of the digital resources in a sigma-delta ADC, both the input signal generation and output response analysis are performed on chip. For the purpose of BIST, a 4th order decimation filter of the sigma-delta ADC has been used instead of a 3rd order in the non-BIST case. In this case, more digital hardware is required to implement the filter.

A nonlinear ramp signal is applied to ADCs for static testing in [Vor10]. The basic idea is that the most linear segment of a nonlinear ramp signal is identified and employed as the test stimulus. In the conventional test method, the amplitude of the ramp signal is the same as the input range of the ADC under test. In contrast, the proposed test method requires the amplitude to have multiple times the input range of the ADC. It is validated by the experimental results of two 8-bit and one 10-bit ADC.

A staircase-like exponential waveform can be generated by a pulse-width modulated (PWM) signal followed by an off-chip RC filter to test the 3rd harmonic distortion of the ADC [Roy02]. The simulation results predict that the test stimulus is suitable for ADCs up to 20-bits, and is primarily limited by the linearity of the off-chip capacitor.

The authors in [Ven07] described an approach to test the gain, offset, 2nd and 3rd harmonics and SNR of a sigma-delta ADC simultaneously. The results are obtained by only applying a fully binary PWM test signal to the ADC and post processing the digital samples at the output.

A BIST architecture while utilizing the on-chip processor is presented in [Che02]. It uses the RC charging exponential waveform to test the static parameters of an ADC. The test stimulus is generated from a reference voltage, requiring four resistors and one capacitor. However, the generated waveform is quite dependent on process variations.

The references [Jin03, Jin04, Jin05] present an approach using two imperfect ramp signals with constant offset to test a high resolution ADC. A stimulus error identification and removal (SEIR) algorithm is described for relaxing the linearity requirement of the test signal.

This chapter is organized as follows. In section 3.3, the basic features of both sine-wave and pulse-wave will be discussed and compared. The basic concept and the set-up of the methods, which exploiting different forms of pulse-waves to test dynamic parameters of the ADCs, will be explained in sections 3.4 and 3.5. Subsequently, the simulation results of a 6-bit flash ADC and a 12-bit pipelined ADC will be presented in sections 3.6 and 3.7 respectively. In section 3.8 the measurement results of the 12-bit pipelined ADC will be shown. Finally, the conclusion will be provided in section 3.9.

3.3 Comparison of sine-wave and pulse-wave input stimuli

As introduced in previous sections, the conventional approach of ADC dynamic testing is to use a sine-wave as test stimulus and subsequently apply FFT analysis to obtain the spectrum of the output. From the spectrum, all dynamic parameters of the ADC can be calculated. The ideal spectrum of a pure sine-wave only contains the fundamental frequency as shown in Figure 3.1a [Smi97]. In contrast, the spectrum of a pulse-wave contains different harmonics. The Fourier series of an ideal pulse-wave, $f_{idealpulse}(t)$, can be expressed as:

$$f_{idealpulse}(t) = A*d + \sum_{n=1}^{\infty} \frac{2A}{n\pi} \sin(nd\pi) * \cos(\frac{2n\pi t}{T}) \tag{3.1}$$

where A, d and T denote the amplitude, duty cycle and period, respectively. The symbol n is an integer number. If one assumes that the duty cycle is $1/m$, where m is an integer, then the spectrum of the pulse signal does not contain the multiple of m harmonics. For example if $m=2$, the spectrum of the pulse will only contain the odd harmonics as shown in Figure 3.1b.

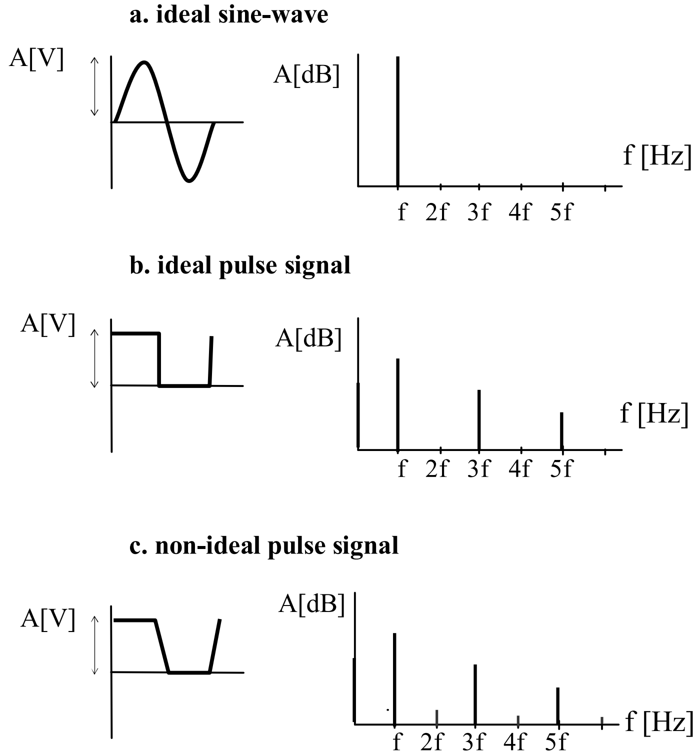

Figure 3.1: The spectrums of the ideal sine-wave, ideal pulse-wave and non-ideal pulse-wave

However, this is only the theoretical case. In practice, the pulse signal will have finite rising and falling edges, which can be expressed in the time domain as:

$$\begin{aligned} x(t) &= \frac{A}{T_r} t\left[u(t) - u(t-T_r)\right] + A\left[u(t-T_r) - u(t-T_r-T_h)\right] \\ &+ A(1 + \frac{T_h + T_r - t}{T_f})\left[u(t-T_r-T_h) - u(t-T_r-T_h-T_f)\right] \end{aligned} \tag{3.2}$$

where A, T_r, T_f and T_h denote the amplitude, rise and fall times and the time the signal is high. The spectrum of an adapted pulse-wave, which is a pulse-wave with rising and falling edges, can be derived as [Smi97]:

$$F\{x(t)\} = \frac{A}{\omega^2 T_r}(e^{-j\omega T_r} - 1) - \frac{A}{\omega^2 T_f}(e^{-j\omega T_h} - 1)e^{-j\omega(T_r + T_h)}$$
$$- \frac{2jA}{\omega^2 T_r}\sin(\omega \frac{T_r}{2})e^{-j\omega\frac{T_r}{2}} - \frac{2jA}{\omega^2 T_f}\sin(\omega \frac{T_f}{2})e^{-j\omega(T_r + T_h + \frac{T_f}{2})} \quad (3.3)$$

ω represents the angular frequency. One can observe that the spectral representation of an adapted pulse-wave is not only a function of the sampling frequency and amplitude of the signal, as for sine-wave stimuli, but also a periodic function of the pulse rise and fall times as well. Compared to a sine-wave, its power spectrum contains other frequency components then one would expect from the fundamental frequency component. Figure 3.1c shows the spectrum of a non-ideal pulse-wave if the duty cycle is 50%.

3.4 Approximation of a sine-wave by using a pulse-wave signal

3.4.1 Duty-cycle settings

From the previous analysis, it was indicated that the spectrum of the pulse signal contains certain harmonics related to its duty cycle. This is the major difference between the power spectrum of a sine-wave and a pulse-wave signal. With a pulse as the test stimulus, its harmonics will be mixed into the output spectrum of the ADC via the inherent nonlinearity of the ADC. Because the harmonics of the pulse itself are quite considerable and difficult to distinguish, they will degrade the accurate measurement results of the dynamic parameters. To solve this problem, we have approximated the sine-wave by an adapted pulse signal. As shown in Figure 3.1b, if the duty cycle is set to d=50% then all even harmonics are zero. Hence, a pulse sequence with different duty cycles can be applied to the ADC to measure the harmonics of its output as shown in Figure 3.2. In this way, the output spectrum approximates the output spectrum of a sine-wave stimulus. It is usually sufficient to take account for six harmonics with regard to dynamic parameters [Bur00]. The specific steps of measuring the harmonics of the ADC are therefore:

Step 1: Set duty cycle d=1/2 of the pulse-wave stimulus. Carry out the FFT calculation to obtain the output power spectrum. Measure the fundamental (H1), 2nd harmonic (H2), 4th harmonic (H4) and 6th harmonic (H6) from the power spectrum.

Step 2: Set d=1/3 of the pulse-wave stimulus and keep the amplitude the same. Rise and fall times and frequency are identical as the pulse-wave in Step 1. Carry out the FFT

calculation to obtain the output power spectrum. Measure the 3rd harmonic (H3) from the power spectrum.

Step 3: Set d=1/5 of the pulse-wave stimulus and keep the other parameters the same as the pulse-wave in Step 1. Carry out the FFT calculation to obtain the output power spectrum. Measure the 5th harmonic (H5) from the spectrum.

Here, all the harmonics are only the approximated values of the ones obtained from a sine-wave stimulus. Although certain harmonics are quite low by setting the duty cycle, other dominant harmonics can be mixed into the corresponding harmonics at the output because of the nonlinearity of the ADC. The magnitudes of the fundamental frequencies are also different with different duty cycles. However, the complexity of the transfer function of the ADC makes it difficult to estimate the relationship between the magnitudes of the fundamental and other harmonics. Therefore, for the following calculation of harmonics we take the fundamental, 2nd, 4th and 6th harmonics measured with d=1/2. The 3rd and the 5th harmonics are measured with d=1/3 and d=1/5 respectively. In summary, the harmonics of the ADCs are obtained from the pulse wave with d=1/2, 1/3 and 1/5.

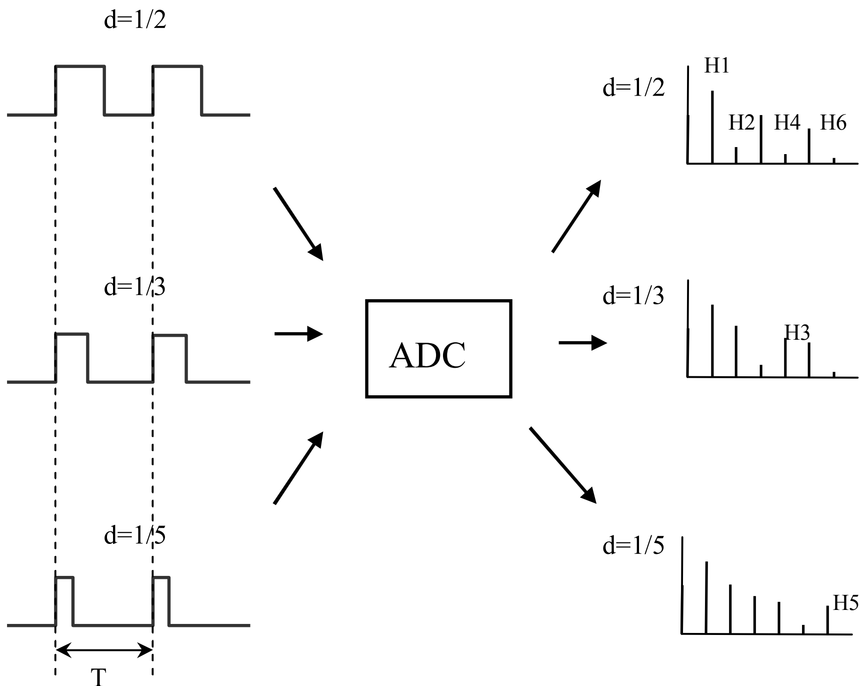

Figure 3.2: The measurement of the harmonics of the ADC by using different duty cycles of the pulse-wave

3.4.2 Rise- and fall-time conditions of the pulse-wave stimulus

If the pulse-wave is exploited for ADC testing, the rising and falling edges are the most crucial parts. In the case of an infinite small rise time (*tr*) and fall time (*tf*) of the pulse-wave stimulus, the output of the ADC will be the digital representation of the low and high levels of the pulse making it unsuitable for performance measurements of the ADC. As result, the rising and falling edges provide the most useful information for ADC testing. They should be sampled in a proper way. If one assumes the sampling frequency of the ADC under test is f_s, the rise and fall time should satisfy the requirement as:

$$tr \text{ and } tf > \frac{1}{f_s} \tag{3.4}$$

This requirement must always be satisfied when testing the ADC with a pulse-wave

stimulus in the remainder of this thesis.

3.5 Multi-level pulse-wave for ADC testing

In section 3.3, a sine-wave is approximated by a set of pulse-waves with different duty cycles. Another potential approach for approximating the spectrum of a sine-wave is adjusting the shape of a digital input stimulus. A sine-wave can be considered as a stair-case pulse-wave with infinite number of voltage levels. A pulse-wave with 3 different voltage levels is shown in Figure 3.3 as an example. The more voltage levels in a stair-case pulse-wave, the more the spectrum of the pulse-wave will be similar to the one of a sine-wave. The spectrum of the pulse-wave of different levels with ideal rise and fall edges is shown in Figure 3.4. One can observe that the levels of the harmonics of the 4-level pulse-wave are mostly below the ones of the 2-level and 3-level pulse-waves. Compared to a 2-level pulse-wave input stimulus, the output spectrum of the multi-level pulse-wave is more close to the sine-wave. In this case, one can expect that the output spectrum from a 3-level and 4-level pulse-waves test stimulus can detect the parametric faults in a more sensitive way as compared to its binary counterpart. Nowadays, most of the ADCs are integrated into a platform-based design. In general, there are multiple power-supply levels (usually at least three levels) in a platform design (analogue, digital, I/O). In this case, it provides the potential to generate a pulse-wave with different levels. Compared with generating an accurate analogue sine-wave on-chip, a stair-case pulse-wave is easier and less expensive to generate in such a kind platform-based design. At first, the stair-case pulse-wave with multiple levels is applied to both golden devices and the DUTs as the test stimulus. The output spectrum can be obtained subsequently via FFT analysis. As a starting point, the most typical dynamic parameter THD is calculated from the output spectrum. It can be obtained for both golden devices and DUTs. By comparing the THD values between the golden devices and the DUTs, the devices having a faulty THD can be distinguished. In [Roy02], a stair-case waveform is also applied for measuring the 3rd harmonic distortion of an ADC. The method is based on a polynomial fitting technique and requires high linearity of the rising and falling slopes of the stair-case waveform. Our method also applies the stair-case pulse-wave. However, the FFT analysis is applied to the output of the ADC for obtaining the THD. As the obtained THD is not sufficiently accurate, it is only exploited to distinguish the devices having a faulty value of the THD.

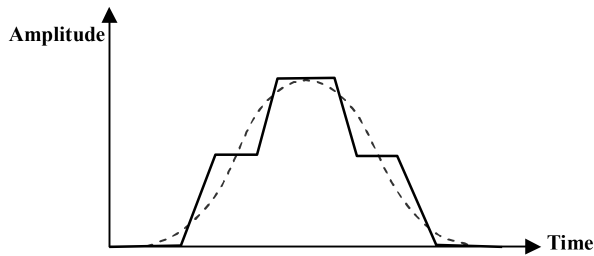

Figure 3.3: The multi-level pulse-wave for ADC testing

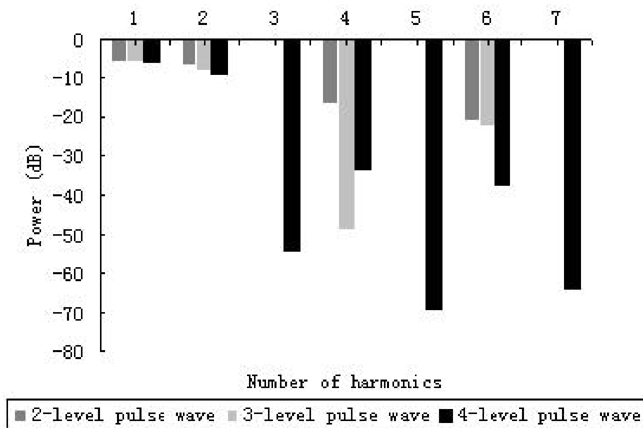

Figure 3.4: The power spectrum of multi-level pulse-waves

3.6 Simulation results and analysis based on transistor-level design of a 6-bit flash ADC

3.6.1 Fault injection strategy of a 6-bit flash ADC

As vehicle for evaluation of the test stimuli testing, the transistor-level design of a 6-bit flash ADC in a 120nm CMOS process has been used [Did04]. As the structure and features of the flash ADC have already been explained in section 2.2.1, it will not be introduced here again.

In our approach, we focus on the parametric faults in the analogue circuitry of the ADC as they are the most difficult faults to detect. The input of the first stage is the input stimulus, while the input of the following stages is amplified and divided into several resolution levels via a resistor-ladder network. Similarly, any faulty behavior in the first stage will be amplified and affect the following stage. As a result, the performance of the A/D converter is the most fault-sensitive in the first stage. In our case, the parametric faults are injected into the first stage, which is composed of 11 pre-amplifiers as shown in Figure 3.5. The first stage pre-amplifiers are randomly chosen and injected with three types of faults respectively, which mainly affect the performance of the first stage:

- Offset fault - by inserting and applying a dc voltage source to the gate of one of the input pair transistors.
- Gain fault - by varying the load resistor value of the amplifier.
- Bandwidth fault - by inserting an extra capacitor at the output of the amplifier.

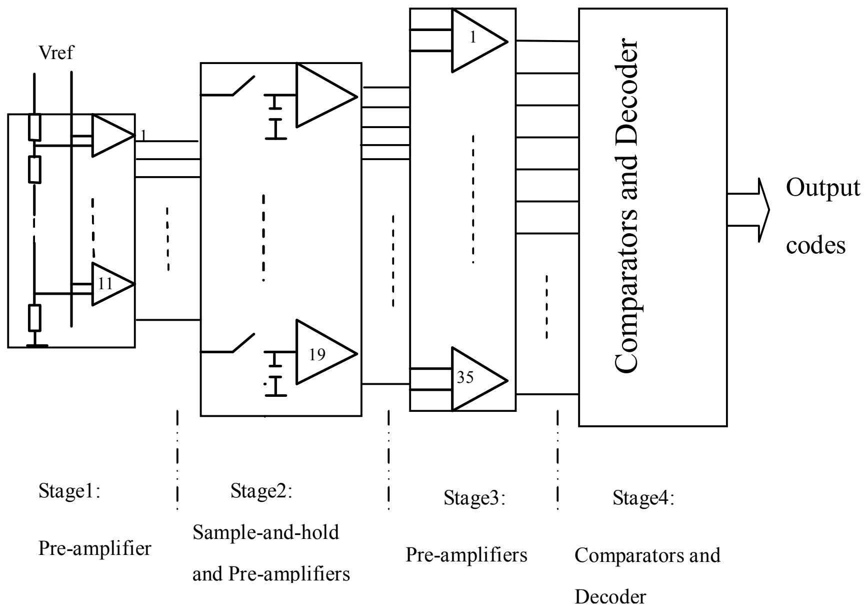

Figure 3.5: The block diagram of a 6-bit flash ADC [Bur00]

3.6.2 Simulating the 6-bit ADC using pulse-waves of different duty cycles as input stimulus

In this section, the 6-bit flash ADC as described in section 3.6.1 is exploited to validate the proposed test method in section 3.4, using pulse-waves of different duty cycles as the test input stimuli. As described in section 3.4, the harmonics will be obtained from the pulse wave with *d=1/2, 1/3 and 1/5*. The noise is obtained from the pulse wave with *d=1/2*. All simulations have been performed with an input frequency f_{in}=7MHz, a sample frequency f_s=300MHz, temperature T=25°C, and a power supply VDD=1.2V. The input pulse wave stimulus is amplitude A=0.46V, offset voltage V=0V. Based on the method proposed in section 3.3, the simulation results of the nominal dynamic parameters and the test conditions are listed in Table 3.1. The simulation results of sine-wave input stimulus are also listed in Table 3.1 as the reference values. One can observe that if the rise and fall times of the pulse-wave are changed from 5ns to 20ns, all dynamic results measured by the pulse-wave are still different from the reference values in the case of a sine-wave input stimulus. Because of the complex transfer function of the ADC, it is rather difficult to obtain an accurate approximated value of the harmonics via a pulse-wave input. In this case, accurate results of the dynamic parameters cannot be obtained from the pulse-wave input signal of different duty cycles.

Table 3.1: Simulation results of dynamic parameters of a 6-bit flash ADC

Parameters @ nominal case	**Sine-wave stimulus**	**Pulse-wave stimulus *tr = 5ns***	**Pulse-wave stimulus *tr = 10ns***	**Pulse-wave stimulus *tr = 20ns***
THD (dB)	-40.5	-39.6	-37.8	-38.9
SNR (dB)	33.2	23.8	26.7	29.5
SINAD (dB)	32.6	38	36.6	38.3

However, our method can still be used as a signature test to distinguish the devices with faulty dynamic parameters if it can reflect the faults of the devices as sensitive as the dynamic parameters. If a pulse-wave is applied as the stimulus, the simulations of all the corner cases

are carried out on the fault-free ADC. Then different values can be obtained for each dynamic parameter. By comparing them, the one representing the worst but still allowed performance of the ADC is selected as the fault-free range.

As discussed in section 3.6.1, three types of faults are injected into the first-stage of the ADC. There are 8 different faulty cases for each type of fault. These 8 different faulty cases are actually the same type of fault but with different values for the relative fault. Figures 3.6 – 3.8 show the results of the dynamic parameters with different type of faults by using the conventional test method. In these figures, the x-axis is the ratio between the faulty and the fault-free values of gain, offset and bandwidth respectively. The fault-free values of gain, offset and bandwidth are obtained from the simulation of the typical case. The y-axis shows the values of the conventional dynamic parameters such as THD, SNR and SINAD. Each point in the curve represents a faulty case. In Figure 3.6, one can observe that if the ratio between the faulty gain and the fault-free gain increases from 0.72 to 0.975, the THD and the SINAD also increase. The curve of the SNR is relatively flat, but actually it shows the same trend as the THD and SINAD. Summarizing, the THD and SINAD become worse as the gain fault increases, while the SNR changes only less than 1 dB.

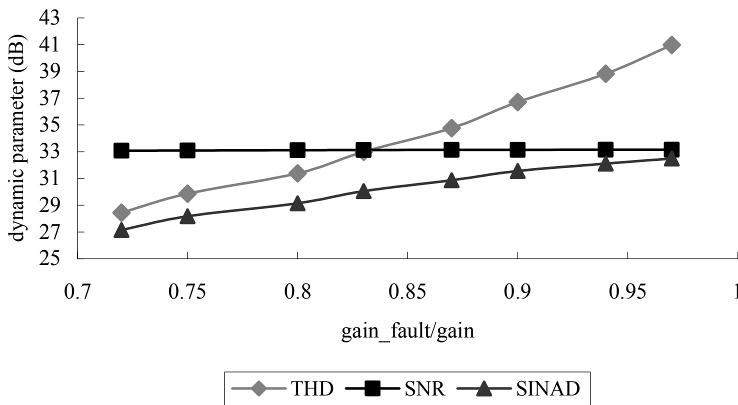

Figure 3.6: The dynamic parameters THD, SNR and SINAD of a 6-bit flash ADC with *gain* ratio faults by using a sine-wave stimulus

Figure 3.7 shows the dynamic parameters versus the injected *offset* fault. As the *offset* fault increases from 2 to 27 times the fault-free offset, the values of the THD, SNR and

SINAD all decrease.

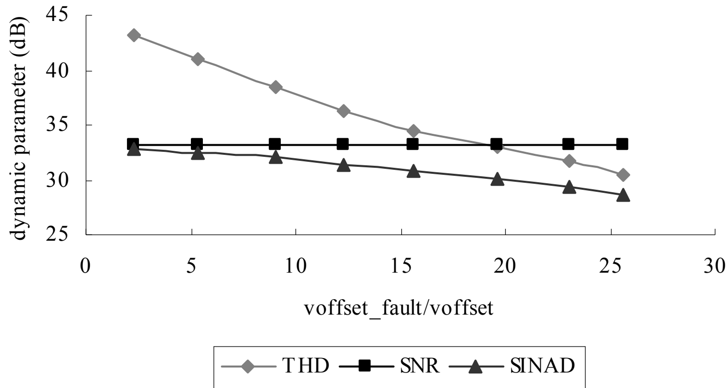

Figure 3.7: The THD, SNR and SINAD of a 6-bit flash ADC with *offset* ratio faults by using a sine-wave stimulus

From Figure 3.7, one can observe that as the ratio between the faulty bandwidth and the fault-free bandwidth increases from 0.028 to 0.078, the performance of the THD, SNR and SINAD becomes better.

From Figures 3.6 - 3.8, one can conclude that if the injected faults (gain, offset and bandwidth faults) are increasing, the dynamic performance of the 6-bit flash ADC becomes worse.

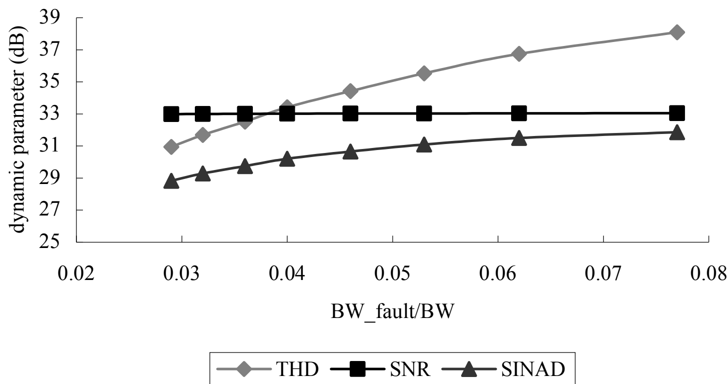

Figure 3.8: The dynamic results of a 6-bit flash ADC with *bandwidth* ratio faults by

using a sine-wave stimulus

A. Total Harmonic Distortion (THD)

In order to determine the THD, the harmonics are obtained by the steps described in section 3.3. The pulse-wave stimuli with 5ns, 10ns and 20ns rise and fall times are applied to the ADC respectively (see Table 3.1). After running the simulation of the corner cases on the fault-free ADC and comparing the results, one can determine that their fault-free ranges are smaller than -39.6 dB, -37.2 dB and -36.7 dB, respectively. They are denoted by the grey dashed lines in Figures 3.9 – 3.11.

- Gain faults of the first-stage amplifiers

The results in Figure 3.9 show the THD values of pulse-wave stimuli with 5ns, 10ns and 20ns rise and fall times respectively. The x-axis denotes the ratio between the faulty gain and the fault-free gain of the amplifiers while the y-axis denotes the THD values. The fault-free range is also denoted by a grey dashed line. Each of them corresponds to the curve of the THD results in the same grey level. The fault-free range is obtained by simulating the fault-free device in the worst case. If a point in Figure 3.9 is out of the fault-free range of the THD, then it is defined as a faulty device by the pulse-wave stimulus approach. From Figure 3.9, one can see that all these three curves have the same trend. As the ratio of the gain increases from 0.72 to 0.97, the THD value of the ADC with a pulse-wave is increasingly closer to the fault-free value. This trend is similar to the THD results obtained by the sine-wave stimulus. It means our method can reflect the gain faults inside of the ADC in a similar way as the conventional method. If the rise and fall times of the pulse-wave are 5ns, 10ns and 20ns respectively, it can detect the 4, 6 and 8 faulty cases respectively. These are represented by the successive dots under the corresponding dashed lines in Figure 3.9.

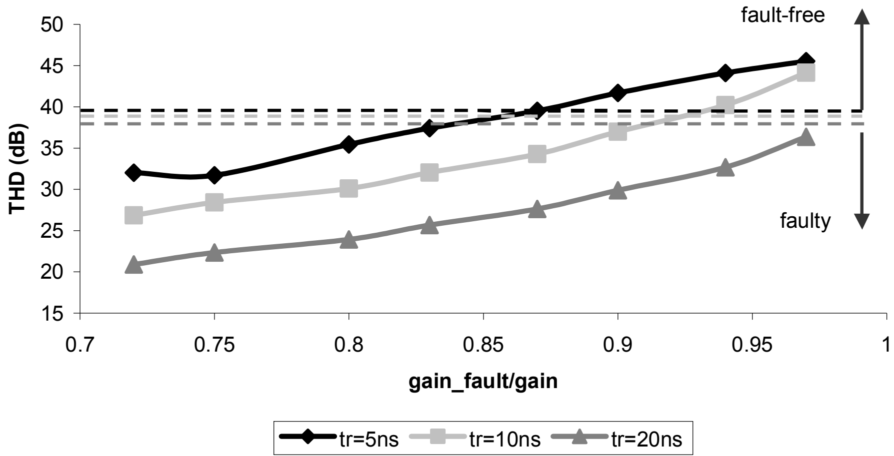

Figure 3.9: The THD obtained by applying a pulse-wave to a 6-bit flash ADC with a *gain* fault in the first-stage amplifier

- **Offset faults of the first-stage amplifiers**

As stated before, another category of faults are offset faults. In Figure 3.10, the x-axis denotes the ratio between the faulty offset and the fault-free offset of the amplifiers while the y-axis denotes the THD values. The fault-free offset is the offset value of the fault-free ADC in the typical case. It can be seen from Figure 3.10 that the three curves have still the same trend. As the offset increases, the THD performance with the pulse-wave input signal becomes worse. Compared to the results obtained by the pulse-wave with different rise times, the larger the rise time the more faulty cases can be detected.

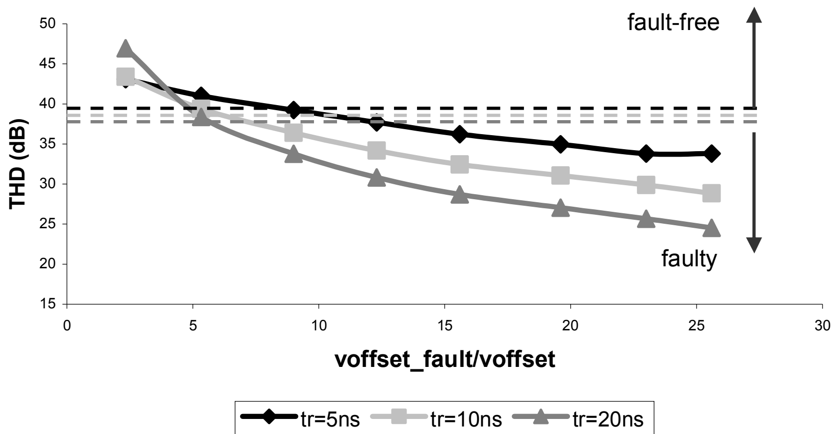

Figure 3.10: The THD obtained by applying a pulse-wave to a 6-bit flash ADC with an *offset* fault in the first-stage amplifier

- **Bandwidth faults in the first-stage amplifiers**

The bandwidth faults are the third type of fault injected into the ADC. The x-axis in Figure 3.11 denotes the ratio between the faulty bandwidth and the fault-free bandwidth of the first-stage amplifiers while the y-axis denotes the THD values. From the results, one can see that the pulse-wave stimulus can detect all the errors. However, if the rise time increases, the distance between the curve and the fault-free range is also larger. This means the pulse-wave with a larger rise time is more sensitive to bandwidth faults.

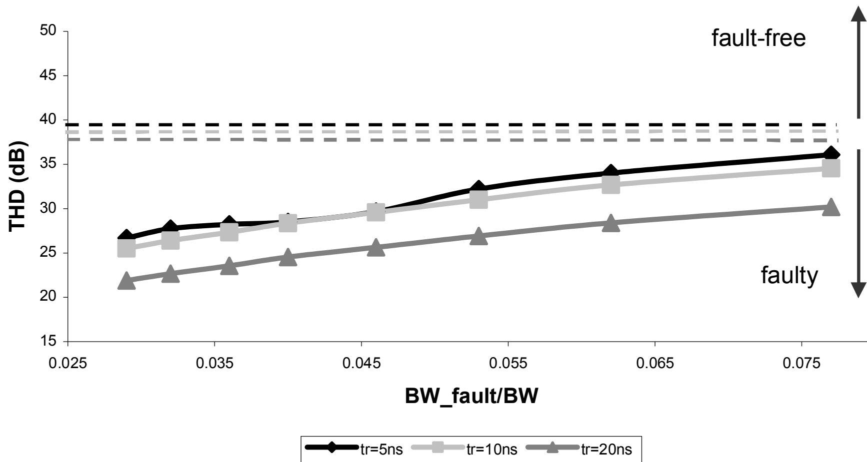

Figure 3.11: The THD obtained by applying a pulse-wave to a 6-bit flash ADC with a *bandwidth* fault in the first-stage amplifier

B. Signal-to-Noise Ratio (SNR)

Because the SNR does not contain the harmonics, only the pulse-wave stimulus with *d=1/2* is used to measure it. From Table 3.1, one can observe that the measurement of SNR by a pulse input stimulus is not as accurate as the value with a sine-wave stimulus. This is because the harmonics of the pulse-wave can be mixed into the noise via the nonlinearity of the ADC. The fault-free ranges of the pulse-wave stimuli are larger than 23.7dB, 26.5dB and 29.4dB with *tr* = 5ns, 10ns, and 20ns respectively (see Table 3.1). Figures 3.12 – 3.14 show the results of the SNR under different types of faults. For all three types of faults, the pulse-wave can only detect the bandwidth fault. The pulse with the large rise time *tr* =20ns can detect more faulty cases than the others.

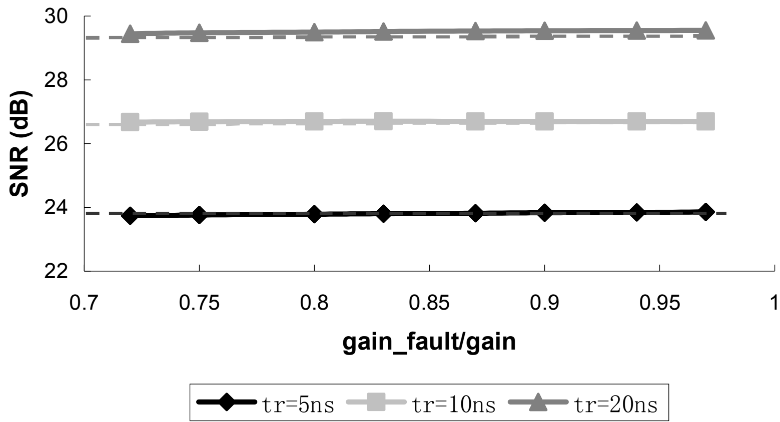

Figure 3.12: The SNR results of a 6-bit flash ADC with *gain* faults in the first-stage amplifier by using the pulse-wave stimulus

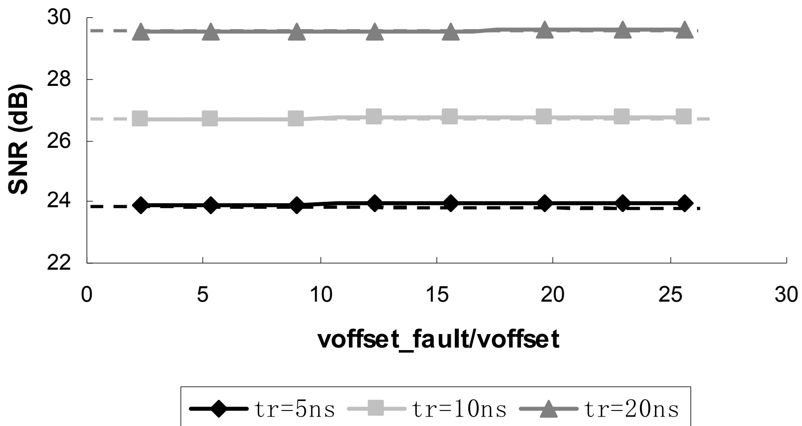

Figure 3.13: The SNR results of a 6-bit flash ADC with *offset* faults in the first-stage amplifier by using the pulse-wave stimulus

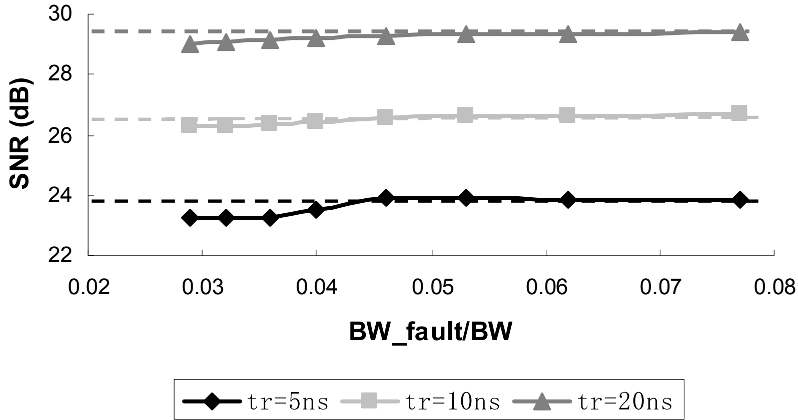

Figure 3.14: The SNR results of a 6-bit flash ADC with *bandwidth* faults in the first-stage amplifier by using the pulse-wave stimulus

C. Signal-to-Noise-And-Distortion (SINAD))

The SINAD is the ratio of the output signal power to the noise plus distortion power, including harmonics, but excluding DC. Based on the results of the harmonics and the noise of THD and SNR, one obtains the results of SINAD in Figures 3.15 – 3.17. The fault-free ranges of the pulse-wave stimuli are larger than 23.6dB, 26.3dB and 28.7dB with *tr = 5ns, 10ns,* and *20ns* respectively (see Table 3.1). It is noticed that a large rise time is able to detect more faulty cases for all different three types of faults.

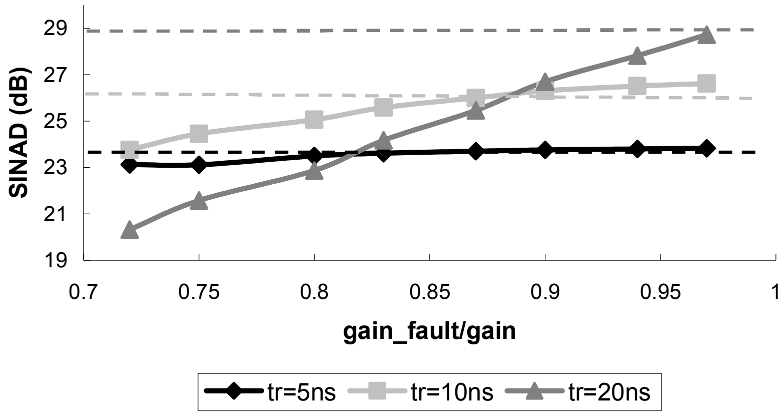

Figure 3.15: The SINAD results of a 6-bit flash ADC with *gain* faults in the first-stage amplifier by applying a sequence of pulse-waves of different duty cycles

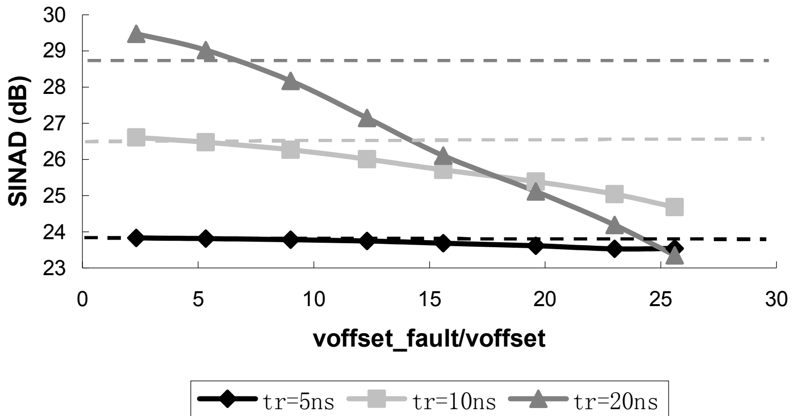

Figure 3.16: The SINAD results of a 6-bit flash ADC with *offset* faults in the first-stage amplifier by applying a sequence of pulse-waves of different duty cycles

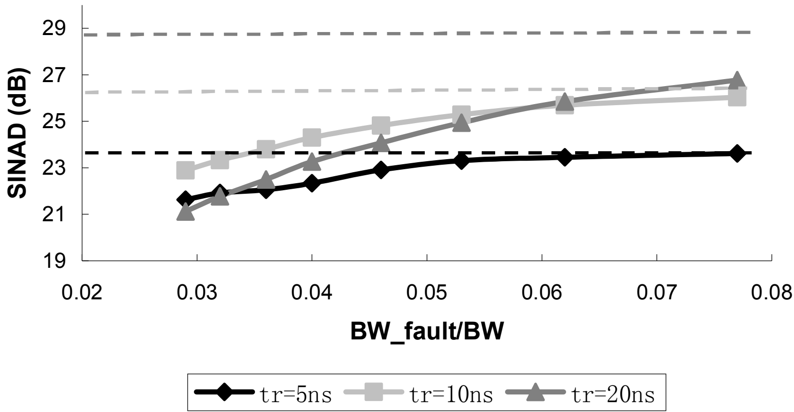

Figure 3.17: The SINAD results of a 6-bit flash ADC with *bandwidth* faults in the first-stage amplifier by applying a sequence of pulse-waves of different duty cycles

Finally, the results shown in Figures 3.6 – 3.17 are summarized in Table 3.2. The number of detected faults with different types of faults and input stimuli are listed in Table 3.2. One can observe that the proposed test method using pulse-wave stimulus with different duty cycles can detect a number of faults in a 6-bit flash ADC. In general, the number of faults detected by the pulse-wave stimuli is less than the one with the sine-wave. As the rise and fall times of the pulse-wave increases, it becomes more sensitive to the faults. It can be seen that when the *tr* and *tf* increase to *20ns*, the pulse-wave input signal can detect nearly as many faulty cases of the THD and SINAD as the sine-wave. However, the ability of detecting the faulty SNR by the pulse-wave is much worse. In the situation of a *bandwidth* fault, 7 faulty cases of the SNR can be found by the pulse-wave while the sine-wave can detect 8 faulty cases. With *gain* and *offset* faults, the pulse signal cannot detect a faulty case of the SNR. Summarizing, for a 6-bit flash ADC, our test method can detect the faulty cases of the THD and SINAD nearly as well as the sine-wave test method. However, this conclusion cannot be applied to other types of ADC.

Table 3.2: The number of detected faulty cases with different types of faults and input stimuli for a 6-bit flash ADC

Dynamic parameters	Types of faults	Sine-wave stimulus	Pulse-wave stimulus *tr=tf*=5ns	Pulse-wave stimulus *tr=tf*=10ns	Pulse-wave stimulus *tr=tf*=20ns
THD	Gain	7	4	8	6
	Offset	6	5	6	6
	Bandwidth	8	8	8	8
SINAD	Gain	7	3	6	8
	Offset	6	2	6	6
	Bandwidth	8	7	8	8
SNR	Gain	8	0	0	0
	Offset	4	0	0	0
	Bandwidth	8	4	4	7

3.6.3 Test of a 6-bit ADC using multi-level pulse-waves

In a next experiment three pulse-waves with a different number of voltage levels have been applied to the ADC respectively. As shown in Figure 3.18, all pulse-waves have the same frequency f_{in}=7MHz. The lowest voltage level V_{low}=-0.46V while the highest voltage level V_{high}= 0.46V. The sampling frequency of the ADC is *300 MHz*. The total rise or fall time is *tr* or *tf= 30ns*. In order to investigate only the impact of the number of levels of the pulse-waves, the total rise and fall times are kept the same. As result, the rising and falling edges of the three pulse-waves in Figure 3.18 are set as follows:

- If the pulse-wave has *two* levels, the rise time is tr_1=30ns and the fall time is tr_1=30ns.
- It is assumed the rise (tr_2) and fall (tf_2) times of each level are equal to the pulse-wave with *three* levels. The total rise time is $tr_2+tr_2=30ns$ and the total fall time is $tf_2+tf_2=30ns$.

- The pulse-wave with *four* levels has identical rise (tr_3) and fall (tf_3) times of each level. The total rise time is $tr_3+ tr_3+ tr_3=30ns$ and the total fall time is $tf_3+ tf_3+ tf_3= 30ns$.

The results of the THD values with gain faults of the first-stage pre-amplifier are shown in Figure 3.19. The x-axis indicates the ratio between the faulty gain and the fault-free gain, while the y-axis denotes the THD values of the ADC output obtained by applying the multi-level pulse-waves. The three curves in different grey levels represent the results by those three different types of pulse-waves shown in Figure 3.18 respectively. One can observe that if the number of voltage levels increases, the change of the THD value by the gain faults is more obvious. This means the THD results can reflect the faults in a more sensitive way.

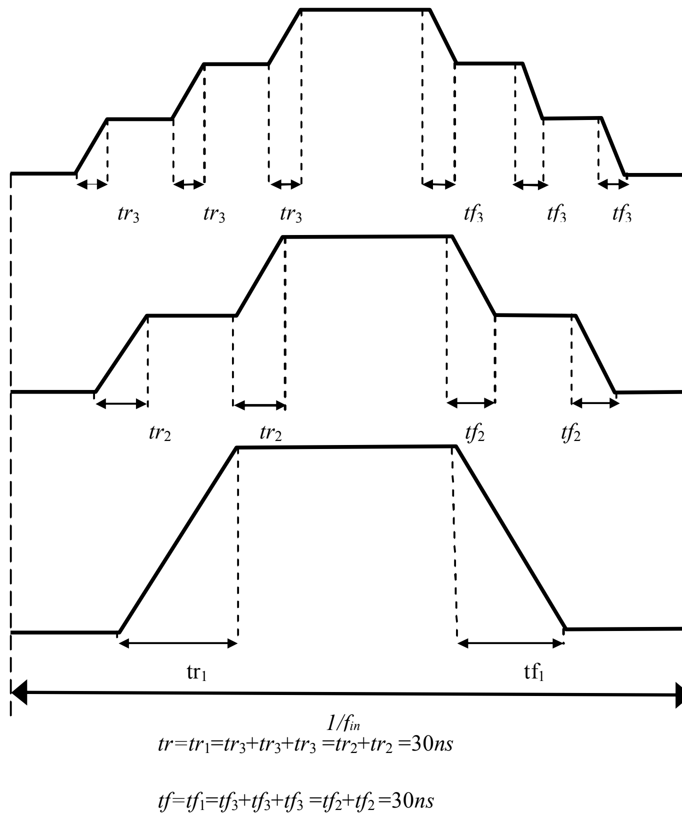

Figure 3.18: Setup of multi-level pulse-wave

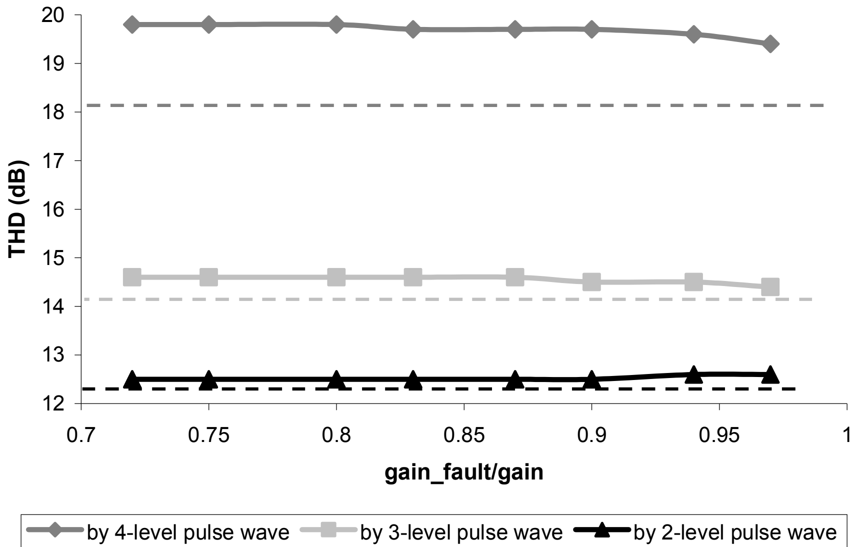

Figure 3.19: The THD obtained by the multi-level pulse-wave for a 6-bit flash ADC with *gain* faults

The results of the THD values with offset and bandwidth faults are shown in Figures 3.20 and 3.21 respectively. In this case, the increase of the number of voltage levels does not affect the results as obvious as it does in the case of gain faults.

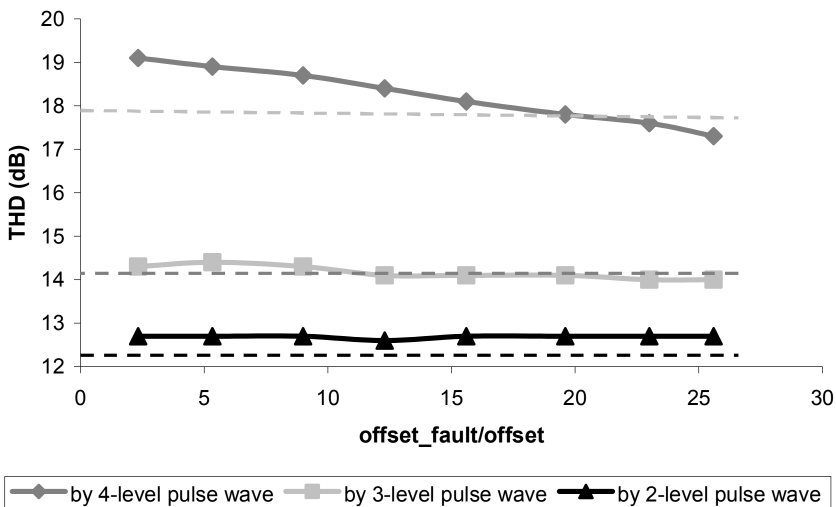

Figure 3.20: The THD obtained by the multi-level pulse-wave for a 6-bit flash ADC with *offset* faults

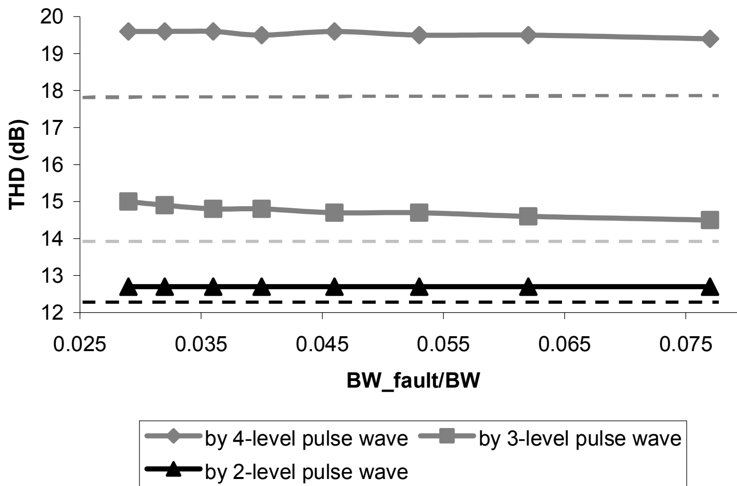

Figure 3.21: The THD obtained by the multi-level pulse-wave for a 6-bit flash ADC with *bandwidth* faults

Table 3.3: The number of detected faults with sine-wave and multi-level pulse-wave stimuli for a 6-bit flash ADC

Types of faults	Sine-wave stimulus	2-level pulse-wave stimulus	3-level pulse-wave stimulus	4-level pulse-wave stimulus
Offset fault	6	0	5	6
Gain fault	7	0	0	0
Bandwidth fault	8	0	0	0

After running the simulations with all three types of faults respectively, the results from the different types of input stimuli are shown in Table 3.3. In each type of fault, 8 different faulty cases are injected in total. The number of faulty cases which are detected by the input stimulus is listed in Table 3.3. It shows that with the gain and bandwidth faults in the

first-stage amplifier, the sine-wave input stimulus can detect the faults far better than all the other pulse-wave input stimuli. However, with offset faults, the 3-level pulse-wave input signal can detect the fault as well as the sine-wave input signal. The 4-level pulse-wave is even more sensitive to the offset fault than in the case of the sine-wave. It can detect 6 faulty cases while the sine-wave can only detect 5 faulty cases. In general, the multi-level pulse-wave is only sensitive to the offset faults.

Compared the results of Table 3.2 with the ones of 2-level pulse wave in Table 3.3, the pulse wave can obtain much better fault coverage in Table 3.2. The reason is that in these two tables we used completely different stimulus. In Table 3.2, the harmonics are all obtained from the pulse wave with d=1/2. While, in Table 3.2 only the 1st, 2nd, 4th, and 6th harmonics are obtained from the pulse wave with d=1/2. The 3rd and the 5th harmonics are from the pulse wave with d=1/3 and 1/5. As we explained in section 3.3, the duty cycle of the pulse wave can significantly affect its spectrum. That is the reason the difference of the THD results between Table 3.2 and 3.3.

3.7 Simulation results and analysis based on a Labview model of a 12-bit pipelined ADC

3.7.1 A 12-bit pipelined ADC and fault injection

As there is no matching silicon vehicle of the 6-bit flash ADC to carry out actual measurements, a 12-bit 80Ms/s pipelined ADC has been selected as the target device to validate our method. As its structure and features have already been introduced in Chapter 2, they will not be explained in this section anymore.

Part of its data sheet related to our simulations and measurements is shown in Table 3.4. In the data sheet, when the input frequency (f_{in}) is 1.8MHz and sampling frequency (f_s) is 50MHz, the minimum, typical or the maximum values of the dynamic parameters are provided. The allowed supply voltage ranges from 1.1 V to 1.3V.

Table 3.4: Part of the data sheet of the 12-bit pipelined ADC

Parameters	f_{in} (MHz)	f_s (MHz)	Min	Typical	Max
Supply voltage (V)	-	-	1.1	1.2	1.3
THD (dB)	1.8	50	-	-75	-65
SNR (dB)	1.8	50	62	64	-
SINAD(dB)	1.8	50	60	63	-

For simulations, this 12-bit pipelined ADC is modeled at the behavioral level using the program Labview. The architecture of this 12-bit ADC is shown in Figure 2.2, on which the Labview model of the ADC is based. In the Labview model, the parameters of each sub-stage of the ADC can be tuned in the simulation. Examples are the gain, the offset, the mismatch of capacitors of the MDAC and so on.

In the provided Labview model of the 12-bit pipelined ADC from NXP, several key parameters that can affect the performance of the ADC have been included [Pla94]:

- The reference voltages of the comparators in the flash ADC of each sub-stage
- The values of the capacitors in the MDAC of each sub-stage
- The gain of the residue amplifier in the MDAC of each sub-stage

In order to validate our method, the faulty 12-bit pipelined ADCs are required in both the simulations and measurements. Unfortunately, there was no faulty ADC available for the measurements. Therefore, the faulty devices need to be emulated by fault-free devices. There are several ways to emulate faulty devices. For better analysis of the simulation and measurement results, the way of fault injection in the simulation has to be the same or related to each other between simulation and measurement. Because the accessibility of the real-life ADC under test is limited, we finally found that changing the supply voltage in the measurements is the simplest way to emulate a faulty device. As described before, there are three key parameters in the model but only the gain of each sub-stage is related to the supply voltage [Mar98]. As a result, only the gain fault of the residue amplifier has been injected into the Labview model to emulate the change of the supply voltage in the measurement.

Since most residue amplifiers in a pipelined ADC use an operational amplifier (op-amp) [Kim04], a simulation on a transistor-level design of a normal folded cascode op-amp with gain boosting has been carried out [Bul90]. It shows the relationship between the gain and the supply voltage of an op-amp. The simulation results are shown in Figure 3.22. One can observe that in the case the supply voltage decreases from 1.5V till 1.1V, the gain of the amplifier slowly decreases. If the supply voltage decreases below 1.1V, which is the lowest allowed supply voltage required for the amplifier, the gain of the amplifier drops very fast. As a result, for the simulation of the 12-bit ADC, 10 different values of the gain are selected, which decrease from 65dB to 42.5dB. When the gain value is between 60 and 65 dB, the op-amp operates as a fault-free device. If the gain is below 60 dB, it operates as a faulty device. In this way, both the faulty and fault-free devices are emulated in our simulations. In the simulation, the gain error injected in each sub-stage of the ADC is the same. Obviously, the gain error is different from stage to stage in real life. However, because we cannot change the supply voltage per stage, it has been assumed they are the same for easier investigation and analysis.

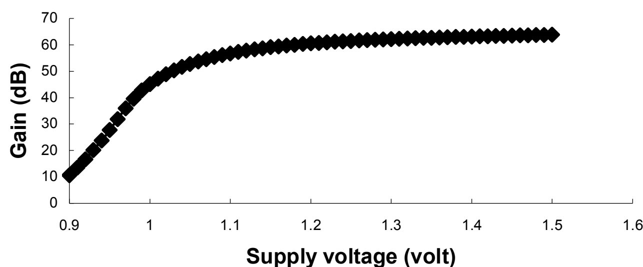

Figure 3.22: Simulated gain vs. supply voltage of a cascode op-amp with gain boosting

Figure 3.23 shows Labview simulation results of the conventional dynamic parameters if the gain of every residue amplifier of the pipelined ADC decreases. As can be seen in Figure 3.23, the dynamic performance degrades as the gain decreases. According to the specification of the 12-bit pipelined ADC, the fault-free range of the THD, SNR and SINAD are above 65dB, 62dB and 60dB. From Figure 3.23, one can notice that the THD, SINAD and SNR become faulty when the gain is below 60dB, 57.5dB and 52.5dB respectively.

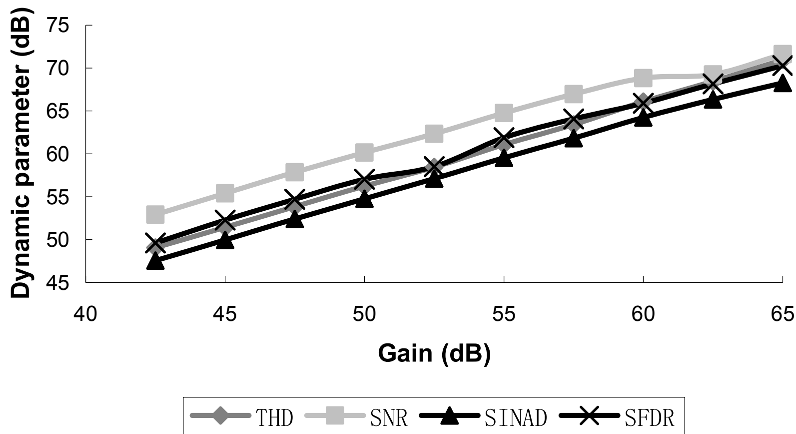

Figure 3.23: Dynamic parameters vs. gain of each sub-stage of the 12-bit pipelined ADC in Labview simulation

3.7.2 Simulation of a 12-bit ADC using pulse-wave stimuli of different duty cycles

In order to investigate the influence of the rise and fall times of the input stimulus, different values of them have been used in the pulse-wave input signal respectively. The setups of both the conventional ADC test method and our own test method in terms of simulation parameters are shown in Table 3.5. In the table, f_{in} indicates the input frequency, *Ns* denotes the number of samples, f_s is the sampling frequency and *tr* or *tf* is the rise or fall time. One can see that only the rise and fall times are different from each other in the setups of using an input pulse-wave.

Table 3.5: The setups of Labview simulation with pulse-waves of different duty cycles

Input stimulus	f_{in} (MHz)	*Ns* (#)	f_s (MHz)	Duty cycle (%)	*tr/tf* (ns)
Sine-wave	1.8	16384	50	-	-
Pulse-wave 1	1.8	16384	50	20/33/50	25
Pulse-wave 2	1.8	16384	50	20/33/50	50
Pulse-wave 3	1.8	16384	50	20/33/50	100

The testing method is exactly the same as the one applied for the 6-bit flash ADC. The results are shown in Figures 3.24 – 3.26. In these figures, the x-axis denotes the gain of the sub-stage while the y-axis denotes the dynamic parameters by applying the pulse-wave stimulus of different duty cycles. The dashed line denotes the boundary of the fault-free range. Each of them corresponds to the curve in the same grey level. The fault-free ranges for THD, SINAD and SNR are the values of the dynamic parameters if the gain is 60dB, 57.5dB and 52.5dB respectively.

In Figure 3.24, the gain of each of the sub-stages decreases from 65dB to 42.5dB. The THD also increases but with a very small change; it is less than 1 dB for all three different setups. Compared with the THD results in Figure 3.23, the change in the curve is much less. Therefore, the THD obtained by using pulse-wave stimuli of different duty cycles is much less sensitive than the one obtained by the conventional test method. From the SNR and SINAD results in Figures 3.25 and 3.26, it can be seen that the SNR and SINAD also increase with a very small value as the gain decreases.

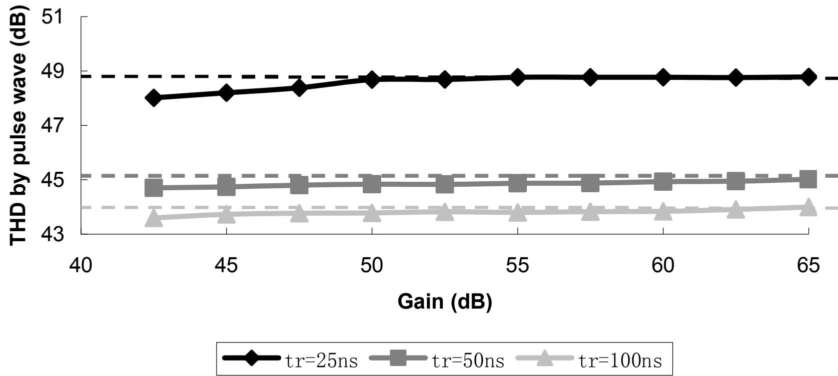

Figure 3.24: Simulation results of the THD in a 12-bit pipelined ADC using a pulse-wave input of different duty cycles

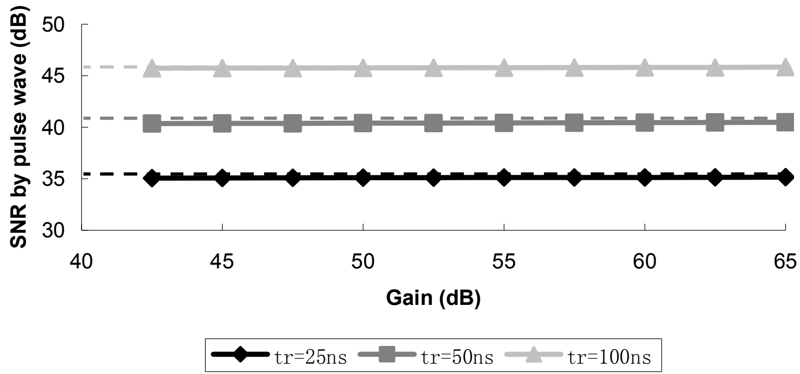

Figure 3.25: Simulation results of SNR in a 12-bit pipelined ADC using pulse-wave input of different duty cycles

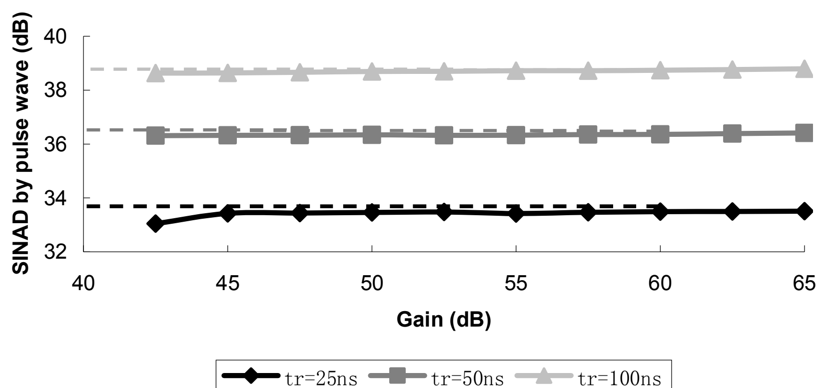

Figure 3.26: Simulation results of SINAD in 12-bit pipelined ADC using pulse-wave input of different duty cycles

Table 3.6 shows the number of fault detections with sine-wave and pulse-wave stimuli. It is observed that the pulse-wave input stimulus can detect the faults as good as the sine-wave in most of the cases. The worst results are under the condition *tr* =25ns, where there are 2 faulty cases for THD and 1 faulty cases for SNR being missed by the pulse-wave input stimulus. However, Figures 3.24 – 3.26 show that the deviation of the dynamic results obtained by our method is very small. In a real test environment it will require very accurate measurements.

Table 3.6: The number of detected faults by using sine-wave and pulse-wave of different duty cycles for a 12-bit ADC in Labview model

Dynamic parameters	Sine-wave stimulus	Pulse-wave stimulus *tr=tf=25ns*	Pulse-wave stimulus *tr=tf=50ns*	Pulse-wave stimulus *tr=tf=100ns*
THD	7	5	7	7
SINAD	6	6	6	6
SNR	4	3	3	4

3.7.3 Simulation of a 12-bit ADC using pulse-waves of multi-levels

Similar to the pulse-wave shown in Figure 3.18 for simulation of the 6-bit flash ADC, three pulse-waves with different levels have been applied to the 12-bit pipelined ADC as test stimulus respectively. All pulse-waves have the same input frequency f_{in} =1.8MHz, the total rise (*tr*) or fall (*tf*) time being 60ns. The lowest voltage level V_{low} is -0.99V and the highest voltage level V_{high} is 0.99V. The sampling frequency (f_s) of the ADC is 80MHz and the number of samples (N_s) is 16384.

Table 3.7: Number of detected THD faults of a 12-bit ADC Labview model with sine-wave and multi-level pulse-wave stimuli

Type of input stimulus	2-level pulse-wave stimulus	3-level pulse-wave stimulus	4-level pulse-wave stimulus	Sine-wave stimulus
# of detected THD faults	3	7	7	7

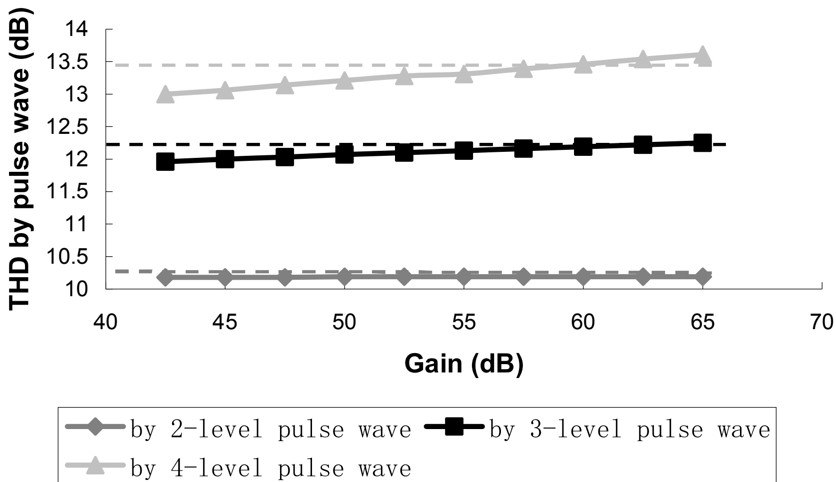

Figure 3.27: The THD simulation results of 12-bit pipelined ADC using the multi-level pulse-wave as input stimulus

The simulation results are shown in Figure 3.27. The x-axis is the value of the gain of each sub-stage while the y-axis is the THD obtained by using multi-level pulse-wave. The dashed line is the fault-free range of the THD. The expected result is that the THD, while using the pulse-wave with more voltage levels, is closer to the trend of the actual THD as shown in Figure 3.23. From Figure 3.27, one can see that the curve of the results obtained by the 2-level pulse-wave is the most flat while the one obtained by the 4-level pulse-wave has the steepest slope. This means the THD results obtained by the 4-level pulse-wave are most sensitive to the gain faults. The number of detected faulty cases of both sine-wave and multi-level pulse-wave stimuli are listed in Table 3.7. It can be seen that the 3-level and 4-level pulse-waves can detect as many faulty cases as the sine-wave, while the 2-level pulse-wave can only detect 3 faulty cases.

3.8 Measurement setup and results of a 12-bit pipelined ADC

3.8.1 Overview of the Aqua chip

In order to evaluate our method on a silicon vehicle, a 12-bit pipelined ADC integrated in the analogue qualification test chip (Aqua) of NXP has been selected as the target device. The Aqua chip is a combined analogue test chip including several analogue blocks, which is used for silicon qualification of analogue IPs of NXP. The analogue blocks in the Aqua chip contain ADCs, DACs, oscillator, PLL, signal generators and so on. Compared with a separate test chip for each analogue block, it has several advantages:

- Integrating analogue blocks into one test chip is more cost effective than a separate chip for each IP.
- The performance of the analogue blocks at system level can be tested (e.g. combination of oscillator, PLL and ADC).
- Since ADCs and DACs are often integrated into the same chip, it is possible to construct a loopback testing set-up using only digital I/O. Furthermore it is possible to measure the jitter performance of PLLs or oscillators by using the on-chip ADCs and DACs. This allows the chip to be tested on a tester with limited analog capabilities.
- A combined analog qualification chip can be used to monitor the manufacturing process.

The 12-bit pipelined ADC in this Aqua chip is designed in CMOS 65nm process operating at a power supply of 1.2V. All the following measurements have been carried out on the pipelined ADC integrated in the Aqua chip.

3.8.2 Measurement results and analysis

3.8.2.1 Measurements on a 12-bit pipelined ADC using a pulse-wave with different duty cycles

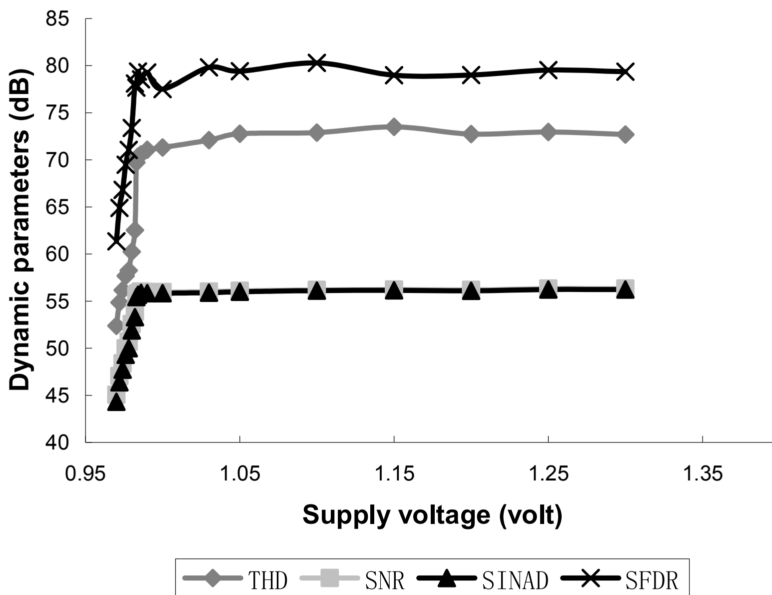

Figure 3.28: Conventionally measured dynamic parameters of a 12-bit pipelined ADC vs. supply voltage

In the measurements, faulty devices are required to validate the test methods. However, there are no faulty devices available. As discussed in section 3.7.1, they are emulated by changing the supply voltage level of the ADC in order to relate the fault injection in the simulation. The dynamic parameters of the ADC with different supply voltage levels are shown in Figure 3.28. They are measured by using a conventional sine-wave and the used test setup is listed in Table 3.5. For each supply voltage setting, the measurement is repeated 10 times. In Figure 3.28, the value of each point is the average of 10 measurement results.

Compared with the dynamic specification in Table 3.4, the SNR and SINAD results are worse than the specification even if the supply voltage has the typical value 1.2V. In the standard setup of the 12-bit pipelined ADC measurement a low pass filter is connected between the input sine-wave and the ADC under test to filter out noise. However, if a pulse-wave is applied as the test stimulus, a low-pass filter will seriously round the rising and falling edges. In this case, the filter cannot be used if a pulse-wave is the input signal. In order to compare the results between the sine-wave and the pulse-wave stimuli, the measurement setup without a low-pass filter is applied to both cases. As a result, the noise of the input signal increases and the SNR and SINAD results become worse.

It can be observed that the curves of the dynamic parameters are relatively flat from 0.99V to 1.3V. Below 0.99V, the values of the dynamic parameters drop very fast. As the supply voltage in the specification of the ADC ranges from 1.1V to 1.3V, the fault-free ranges of all the dynamic parameters are defined as the measurement values by operating the ADC from 1.1V to 1.3V.

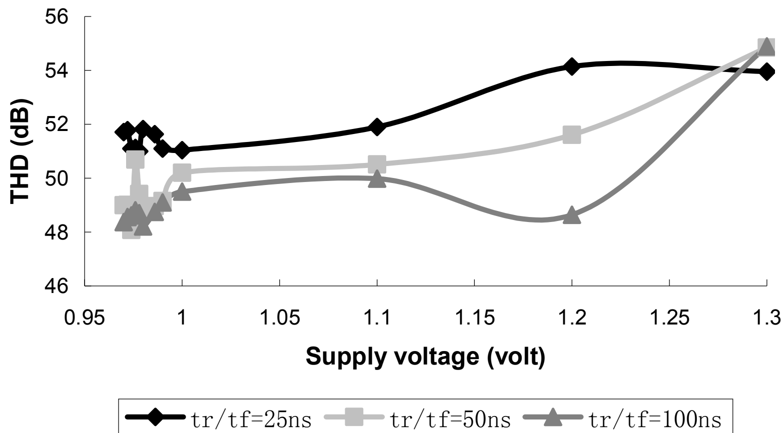

Figure 3.29: Measurement results of THD on a 12-bit pipelined ADC using a pulse-wave of different duty cycles

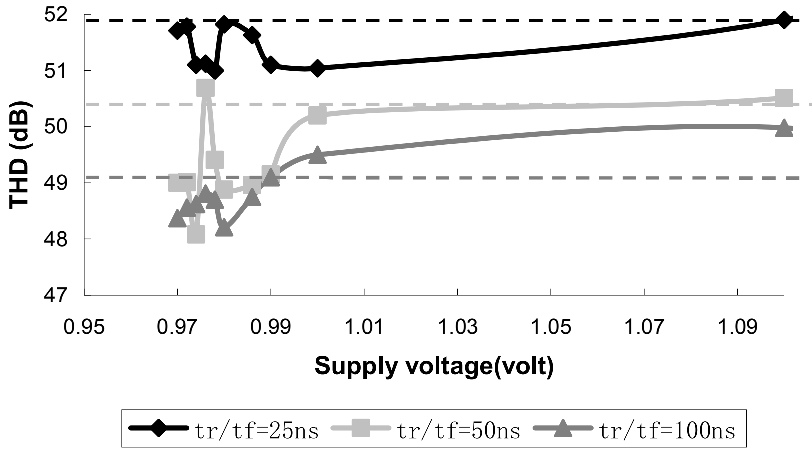

Figure 3.30: The faulty cases of THD on a 12-bit pipelined ADC using a pulse-wave of different duty cycles

The measurement results of the dynamic parameters, which are tested by using the pulse-wave with different duty cycles as input, are shown in Figures 3.29 – 3.34. Figure 3.29 shows the results of the THD while the supply voltage changes from 0.97V to 1.3V. The x-axis denotes the supply voltage while the y-axis denotes the THD with the pulse-wave input stimulus. Compared with the conventional test results in Figure 3.28, the curve of the THD is more flat. As a result, it is less sensitive to faults. In order to see the result of the faulty cases, Figure 3.29 is zoomed in and the results shown in Figure 3.30. It only shows the nine faulty cases as result of changing the supply voltage to 9 different values below 1.1V. The dashed line is the boundary of the fault-free range of the THD with corresponding pulse-wave input signal in the same grey level. If the value of the THD is below the value denoted by the dashed line, then the ADC is defined as a faulty device determined by the method of pulse-wave input stimulus.

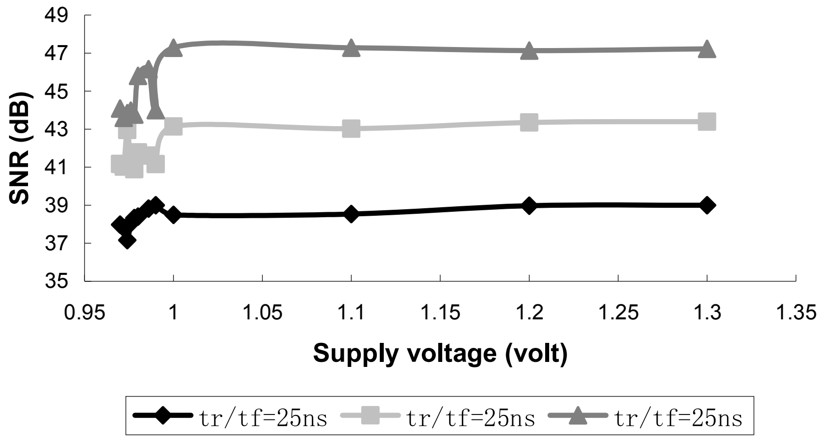

Figure 3.31: The SNR measurement results of the 12-bit pipelined ADC by applying a pulse-wave of different duty cycles

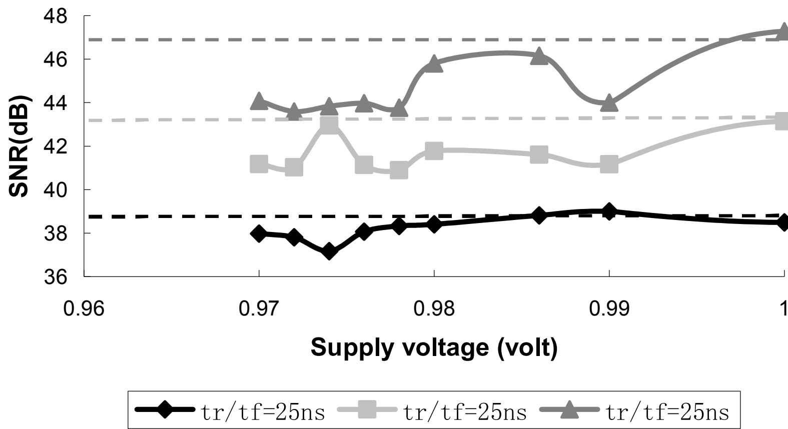

Figure 3.32: The faulty cases of SNR of the 12-bit pipelined ADC using a pulse-wave of different duty cycles

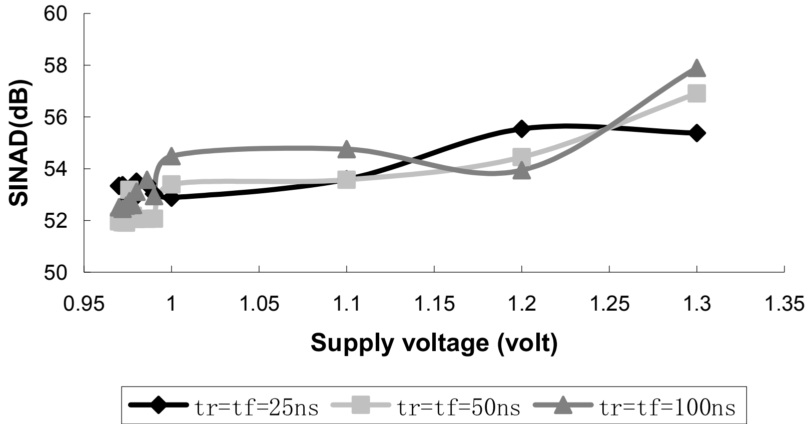

Figure 3.33: Measurement results of SINAD on a 12-bit pipelined ADC by using a pulse-wave of different duty cycles

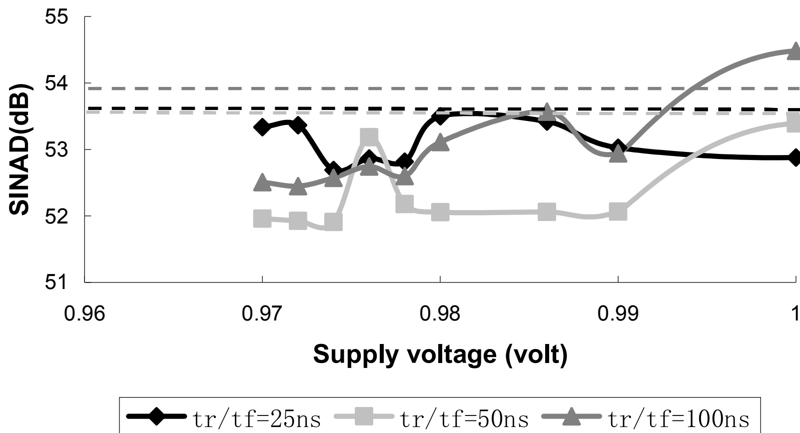

Figure 3.34: The faulty cases of SINAD of the 12-bit pipelined ADC by applying a pulse-wave of different duty cycles

Figures 3.31 and 3.33 show the results of the SNR and SINAD while the supply voltage changes from 0.97V to 1.3V. Similar to the results of the THD, the curves of the results are also more flat as compared to the curve of the conventional (sine) test results. Figures 3.32 and 3.34 are detailed parts of Figure 3.31 and Figure 3.33 respectively. The dashed lines in Figures 3.32 and 3.34 are the same as in the results of the THD, which denote the low limit of

fault-free range.

All the measurement points in Figures 3.29 – 3.34 are the average values of 10 times repeated measurement results. Compared with the conventional dynamic results Figure 3.28, the whole curve of each dynamic parameter is relatively flat. However, one can observe that there are some unexpected bumps in the curves. They can be caused by the inaccuracies of the measurement.

Finally, the number of detected faulty cases of the pulse-wave and sine-wave input stimuli are summarized in Table 3.8. In general, the pulse-wave stimulus with *tr =50ns* can detect the faulty cases better than the other two pulse-waves. It is slightly different from the Labview simulation results, which shows the pulse-wave with *tr =100ns* is as sensitive as the one with *tr =50ns* with respect to the faults. In the simulations, only the gain faults are injected. However, in the measurements, the variation of the supply voltage can cause not only gain faults but also other types of faults. The pulse-wave with longer rise and fall times is not always more sensitive to all the type of faults.

Table 3.8: The number of detected faults with sine-wave and pulse-wave with different duty cycles in the measurements of the 12-bit pipelined ADC based on Figures 3.28-3.34.

Dynamic parameters	Sine-wave stimulus	Pulse-wave stimulus *tr=tf=25ns*	Pulse-wave stimulus *tr=tf=50ns*	Pulse-wave stimulus *tr=tf=100ns*
THD	9	9	8	9
SNR	9	7	9	8
SINAD	9	9	9	8

3.8.2.2 Measurements on a 12-bit pipelined ADC using a pulse-wave stimulus with multiple levels

During these measurements, the input stimuli are multi-level pulse-waves as shown in Figure 3.18, whose input frequency f_{in} is 1.8MHz, while rise (*tr*) and fall (*tf*) times are 60ns as were used in section 3.7.3. The highest and lowest voltages of the multi-level pulse-waves are equal to input range of the ADC. The number of samples *Ns* is 16384 and the sampling

frequency f_s is 50MHz. The measurement results are shown in Figure 3.35. The x-axis is the supply voltage level and y-axis is the value of the THD by using a multi-level pulse-wave input stimulus. Figure 3.36 is the detailed version of Figure 3.35, which only shows the faulty cases. As in the previous figures, the dashed line indicates the low limit of the fault-free range. Compared with the THD results as shown in Figure 3.28, which are obtained by the conventional (sine-wave) test method, the slope of the THD curve is much smaller. The difference between the largest and smallest values of the curve is less than 1dB.

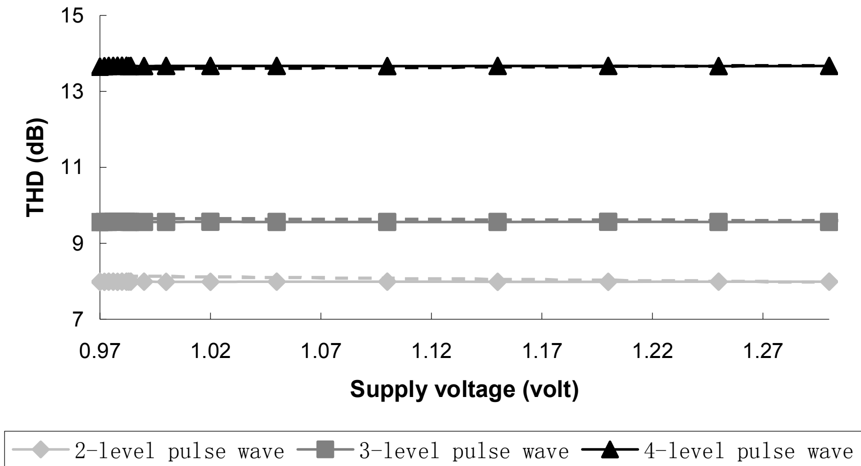

Figure 3.35: The measurement results of THD on a 12-bit pipelined ADC by applying a multi-level pulse-wave

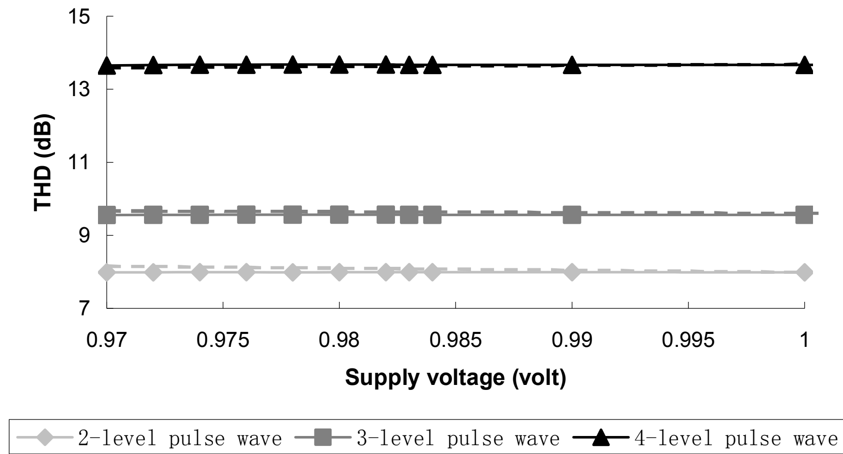

Figure 3.36: The faulty cases of THD on 12-bit pipelined ADC by multi-level pulse-wave

In Table 3.9, the number of detected faulty cases is listed. The results show that increasing the number of levels of a pulse-wave from 2 to 4 can help to improve the test results of a 12-bit pipelined ADC. It is the same conclusion as the one obtained from the Labview simulation results.

Table 3.9: Number of detected THD faults with sine-wave and multi-level pulse-wave stimuli in the measurement of a 12-bit pipelined ADC

Types of input stimulus	2-level pulse-wave stimulus	3-level pulse-wave stimulus	4-level pulse-wave stimulus	Sine-wave stimulus
# of detected THD faults	5	7	7	9

3.9 Conclusions

In this chapter, pulse-waves with different forms have been exploited to test the dynamic parameters of ADCs, which are normally tested by a sine-wave using conventional test

methods. As the spectrums of a sine-wave and a pulse-wave are different from each other, the basic idea in this chapter is emulating the spectrum of a sine-wave by different forms of the pulse-wave. There are two ways to realize this: one is tuning the duty cycles as there is a relationship between the spectrum of a pulse-wave and its duty cycle; the other is increasing the number of the voltage levels of the pulse-wave as it affects the spectrum of the pulse-wave as well. Because of the complexity and nonlinearity of the transfer function of ADCs, these two methods cannot obtain the same accuracy as conventional ADC test methods. However, the results can detect certain faults in the ADC. In this case, they are used to distinguish the devices having faulty dynamic parameters from the devices having fault-free dynamic parameter.

In order to validate these two methods, simulations at transistor-level on a 6-bit flash ADC and at behavioral-level of a 12-bit pipelined ADC have been carried out. For the first method, both simulation results show that the pulse-wave with increased rise and fall times can detect more faults. Compared with the conventional test method, in most of the cases, it can detect the same number of faulty cases. For the second method, in the simulations of the 6-bit ADC, the multi-level pulse-wave can only test the static offset faults. The simulation of the 12-bit ADC shows that the larger the number of voltage levels of the pulse-wave, the more faults can be detected.

As there were no chips available for the 6-bit ADC, measurements have only been carried out with respect to the 12-bit pipelined ADC. For the first method, the results show that the pulse-wave with $tr = 50ns$ obtains the best results for most of the cases. It can detect as many faulty cases as the sine-wave for the dynamic parameters SNR and SINAD. For the THD, it detects one faulty case less than the sine-wave. For the second method, the multi-level pulse-wave can detect more faulty cases with increased number of voltage levels. However, it still cannot detect the faults as well as the conventional methods.

From the measurement and the simulation results, one can see that it is difficult to obtain the dynamic parameters accurately by using a pulse-wave input stimulus. However, with certain settings of the pulse, it can detect the faults of the ADC in an as sensitive way as the sine-wave input stimulus. As it is easier to generate a pulse-wave than a conventional sine-wave input stimulus, it can be used to filter out the faulty devices before the DUTs go through the more complex conventional production testing. In this way, it can save test time and cost.

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Chapter 4

ADC Multi-site Test based on a Pre-Test with Digital Input Stimulus

4.1 Abstract

With the advance of CMOS technology more and more ADCs are integrated into platform-based designs, which are for example used for video, audio and high-speed communication systems. A pulse-wave is obviously easy to generate on such platform-based designs, whose standardized architecture is usually composed of memories, RF and mixed-signal front-ends and increasingly multiple processor cores. In chapter 3, we exploited the adaptive pulse-wave as test stimulus. For post-processing, the output data has only been analyzed in the frequency domain in Chapter 3. However, the measurement results show that it can obtain accurate dynamic results if compared with a sine-wave stimulus. In this chapter, the adapted pulse-wave is still being applied as test stimulus. Two new post-processing algorithms in the *time* domain and one new post-processing algorithm in the *frequency*

domain are proposed. As the test stimulus is relatively easy to generate and post-processing algorithms of the methods are fast, the test is suitable for multi-site testing. The test is proposed as a quick pre-test; filtering out the faulty devices before conventional specification testing. As a result, most of the faulty devices can be filtered out before going to the complicated specification test. Especially if the yield is moderate, it can reduce the production test costs significantly.

4.2 Introduction

As introduced in Chapter 2, the conventional specification tests of an ADC compromise of dynamic and static tests. Typically a dynamic test is for measuring THD, SNR, SFDR, second harmonic and third harmonic power. A static test is to determine INL, DNL, gain and offset. For the specification-based test, a sine-wave or a ramp signal is used to test the dynamic or static parameters. The required quality of test signals depends on the specifications of the ADC under test [Bur00]

Nowadays, multi-site test is a widely used approach in production testing. It can reduce the average testing time per DUT by testing multiple devices on the same tester simultaneously [Vla09]. Nevertheless, for an ADC test, the increasing number of DUTs in parallel usually requires expensive high-quality analogue signal sources. This requirement leads to difficulties in implementing multi-site test with regard to the ADC test [Weg05].

Signature testing for mixed-signal circuits is investigated by many researchers. In this approach, the requirement of the ATE can be relaxed. It will be easier for implementing multi-site test.

In [Yu04], a novel signature for testing mixed-signal circuits is proposed. The signature is generated on-chip based on a Ternary Signal Representation (TSR), which represents the behavior of a signal with three levels being positive, zero and negative. The signature can be exploited to characterize the performance of the ADC and DAC. Based on the TSR, an expensive spectrum analyzer can be avoided.

The work in [Abb09] proposes a signature-based testing for adaptive digitally-calibrated pipelined ADCs. The signature is obtained by integrating the absolute difference between the uncalibrated output and the reference output. The performance of the ADC can be evaluated by using this signature. In this method, the output is captured by low-cost digital circuits, which can relax the requirements of the ATE.

The authors in [Flo03] propose a new method for testing INL and DNL of ADCs. Instead of the conventional test method, white noise is applied as the test stimulus. By analyzing the output spectrum of the ADC, the INL and DNL can be estimated. Compared with a high quality sine-wave or ramp signal, white noise is easier to generate.

This chapter is organized as follows. In section 4.3, the basic concept and steps of the proposed test algorithms are explained. In this section, there are three different test algorithms for obtaining the signature results of the ADCs under test. The simulation results and analysis of the proposed test algorithms of the 6-bit flash ADC are presented in section 4.4. For the 12-bit pipelined ADC, the simulation and measurement results are shown in section 4.5 and 4.6 respectively. In section 4.7, the impact of the impact of the position of the rising edge is investigated on the measurement results. In section 4.8, the comparison between the proposed algorithms and the conventional dynamic test method is presented. Finally the conclusion is given in section 4.9.

4.3 Detection of ADC faults by using a pulse-wave signal

As discussed in Chapter 3, the spectral representation of an adapted pulse-wave is not only a function of the sampling frequency and amplitude of the signal, as for sine-wave stimuli, but a periodic function of pulse rising and falling times as well. As a consequence, its power spectrum contains more redundant frequency components than a sine-wave. If combined with the non-linear response of the ADC under test, well-controlled and accurate determination of ADC's parametric faults via conventional methods become complex and time excessive [She08].

In our case, the time-domain analysis is explored to detect the parametric faults in an ADC with a pulse-wave input signal. Instead of obtaining accurate specification results, a signature result is used to decide whether the DUT passes or fails the test. It is calculated from the time-domain analysis. The basic concept of our method is that by comparing the similarity between the results of the digital outputs of the golden device and the DUT, one can detect faulty devices from a large amount of DUTs in a multi-site test environment. The ideal ADC is perfectly linear and only contains the quantization error, which is determined by the resolution [Pla94]. If the same ideal test stimuli are applied to two ideal ADCs with the same transfer function, their outputs are expected to be the same as well. In the real world, the ADCs with the same design will have similar but slightly different transfer functions, as there are also other types of errors like gain, offset, differential linearity errors and so on, caused by

the fabrication process. Therefore, the transfer functions will differ from the ideal situation as there are additional errors in an ADC. As result, the output will have more variation as well, even with the same ideal input stimuli. In this way, the similarity of the outputs between the golden devices and the DUT can reflect the faults in the DUT. A certain amount of golden devices are used to generate an acceptable range of the output by considering the process variations of the fabrication process. The latter will be discussed later.

A simple and fast pre-test can be carried out by our method before measuring the time consuming specific dynamic and static parameters of the ADC. Most of the faulty devices can be detected by this pre-test and can be discarded from the specification-based tests. Hence the number of devices, which are tested by the complicated and time-costly conventional test, will be reduced. As a result, it will reduce the test time in case a large volume of DUTs needs to be tested. The test flow of this proposed method including both pre-test and ADC specification test is shown as follows:

Step 1: Apply pre-test to all DUTs in a multi-site test environment

Step 2: Discard the faulty devices defined in step 1

Step 3: Apply the specification test to the devices, which pass the pre-test defined in step 1.

The rising and falling edges of the pulse-wave are the crucial parts of the input signal for pulse-wave ADC testing. If a pulse-wave with infinite small rise time (*tr*) or fall time (*tf*) is applied to an ADC, the output of the ADC will be only the digital codes representing the low and high levels of the pulse. Hence it provides too limited information to evaluate the performance of the ADC. The *tr* and *tf* should be at least larger than the reciprocal of the sampling frequency of the ADC [Bur00].

In our algorithms, a modulo-time plot technique [Iro96] is applied to reorganize the output of the ADC to make the time-domain results easier to process. By using this technique, a number of periods of the output are converted into one single period, which still includes the same test information as the original output in the time domain. After applying this algorithm, the output of the ADC is converted from a several-periods pulse-wave into a one-period pulse-wave. The *reconstructed* waveform shows the errors of the ADC more clearly [Iro96]. As an example, the time sequential plot of a pulse-wave sampled by a 6-bit ADC is shown in Figure 4.1. The x-axis denotes the samples in time sequential order, while the y-axis denotes the output amplitude. The frequency of the input pulse signal (f_{in}) is 7MHz, the sampling frequency (f_s) is 300MHz and the number of samples (Ns) is 3002. After

applying the modulo-time plot technique, the reconstructed pulse-wave is shown in Figure 4.2. It clearly shows that the sampled signal is a pulse-wave as in contrast with Figure 4.1.

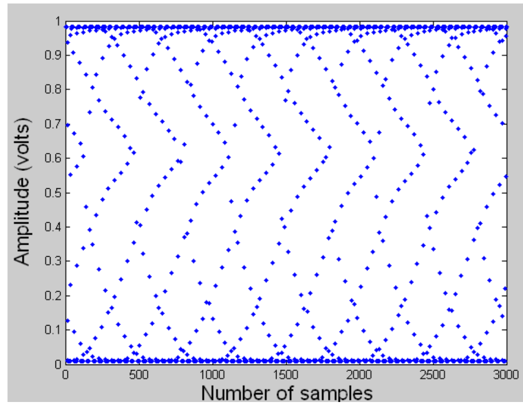

Figure 4.1: The plot of pulse-wave samples in time sequential representation

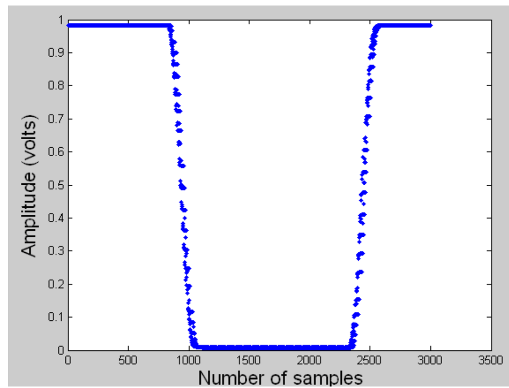

Figure 4.2: The modulo-time plot for the same data as Figure 4.1

4.3.1 Deviation comparison by using the amplitude of the ADC output

In this section, a method for an ADC pre–test is proposed. It is realized by comparing the amplitude of the outputs of the ADCs. The pseudo code of the algorithm used is shown in Table 4.1.

Table 4.1: Overview of the pseudo code of the algorithm comparing the deviation by amplitude (in the time domain)

Algorithm 1: Deviation comparison by amplitude
Initialization
- Initialize the amplitude array *Am* of all sample points for both golden devices and DUT - Initialize the input stimuli
Data collection
- Collect *N* sample points instants for the calculation of each DUT
Main body
1. Calculate the reconstructed output of the golden devices 2. Divide the reconstructed output into four sections and extract the rising or falling edge 3. Obtain the acceptable range of the output amplitude $[Am_{min}(i), Am_{max}(i)]$ 4. Apply step 1 and 2 to all the other DUTs to obtain Am_{DUT} 5. If $Am_{DUT}(i) > Am_{max}(i)$ obtain $\triangle Am(i) = Am_{DUT}(i) - Am_{max}(i)$ If $Am_{DUT}(i) < Am_{min}(i)$ obtain $\triangle Am(i) = Am_{min}(i) - Am_{DUT}(i)$ If $Am_{min}(i) < Am_{DUT}(i) < Am_{max}(i)$ define $\triangle Am(i) = 0$ 6. Increase the index *i*, and repeat previous step for the best estimate 7. Calculate the out-of-range ratio by amplitude *P_am* of each DUT

Initialization and data collection: In order to obtain the fault-free range of the pre-test, a pulse-wave test stimulus is applied to a collection of golden devices with all the corner cases included (such as fast and slow cases). The golden devices are a collection of the samples of fault-free devices defined by the specification test. They are preferably selected from different production lots so that they are a good representation of the process parameter range. Subsequently, the pulse-wave stimulus with identical amplitude, duty cycle, frequency, rising and falling edges will be applied to all the DUTs. Now, a detailed explanation of the

algorithm steps is given:

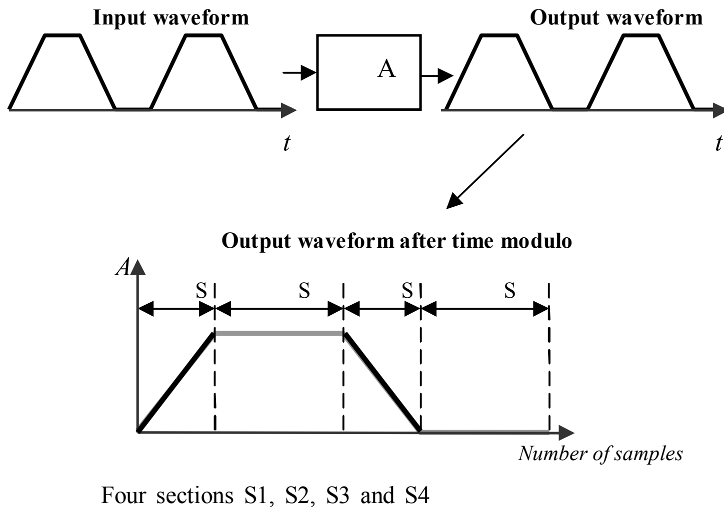

Figure 4.3: Initialization and data collection

Step 1: Apply the technique of the modulo-time plot to the output of the golden devices. After constructing the modulo-time plot, the reorganized output is as shown in Figure 4.3. The x-axis denotes the modulo-time rearrangement of the samples while the y-axis denotes the amplitude of the output. The number of samples can be as many as normally used in conventional (coherent) sine-wave testing.

Step 2: Divide the single-period reconstructed output into 4 sections as shown in Figure 4.3. This is because rising and falling edges of the pulse-wave output contain the most important test information, as compared to the high and low levels. All the golden devices must have the same number of sampling points in each section. For each section, an array of amplitudes *Am* can be obtained where each element *Am(i)* represents the amplitude of one sample point. As discussed before, the rising and falling edges contain the most important test information from the ADCs. For this reason, only the rising or falling edge is employed to calculate the results (S1 and S3 of the pulse-wave in Figure 4.3).

Step 3: Determine the maximum value $Am_{max}(i)$ and minimum value $Am_{min}(i)$ of each element *Am(i)* of all golden devices. They are determined by comparing the values of *Am(i)*

of all the golden devices' outputs.

Step 4: Apply step 1 and 2 to all the other DUTs. When dividing the output into 4 sections, the number of sample points of each section must be the same as in the golden devices. Similar to *Am*, an array of the amplitude Am_{DUT} of the sample points can be obtained from the reconstructed output.

Step 5: The out of range parameter $\triangle Am(i)$ is calculated for each element $Am_{DUT}(i)$ as shown in Figure 4.4. It can be seen that $\triangle Am(i)$ is the absolute distance between $Am_{DUT}(i)$ and the boundary $Am_{min}(i)$ or $Am_{max}(i)$, if $Am_{DUT}(i)$ is not within the acceptable range $[Am_{min}(i), Am_{max}(i)]$. If $Am_{DUT}(i) > Am_{max}(i)$, the amplitude deviation $\triangle Am(i)$ is defined as:

$$\Delta Am(i) = Am_{DUT}(i) - Am_{\max}(i) \tag{4.1}$$

Similarly, if $Am_{DUT}(i) < Am_{min}(i)$, we define the amplitude deviation $\triangle Am(i)$ as:

$$\Delta Am(i) = Am_{\min}(i) - Am_{DUT}(i) \tag{4.2}$$

For the case that $Am_{DUT}(i)$ is within the acceptable range $[Am_{min}(i), Am_{max}(i)]$, the amplitude deviation $\triangle Am(i)$ is defined as 0.

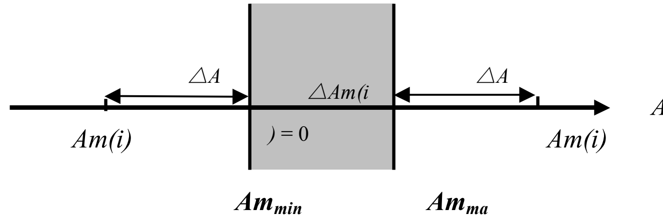

Figure 4.4: The calculation method of the out of range parameter ($\triangle Am(i)$)

Step 6: After collecting the amplitude deviation of all the sample points of each section, the average out-of-range ratio in amplitude *P_am* of each section is defined as:

$$P_am = \frac{\sum_{i=0}^{N} \Delta Am(i)}{\sum_{i=0}^{N} Am_{\max}(i) - \sum_{i=0}^{N} Am_{\min}(i)} \tag{4.3}$$

N denotes the total number of sample points of the rising or falling edge. *P_am* is employed to evaluate the faults in the ADC, which will be shown later on. The numerator in the formula is the sum of out of range parameter $\triangle Am(i)$. The denominator is the tolerance of the output amplitude. By calculating the ratio between them, the *P_am* is anticipated to estimate the faults in the DUT.

4.3.2 Deviation comparison by using the angle of the ADC output

In contrast with the previous algorithm, we now use the angle deviation to evaluate the performance of the ADCs instead of amplitude deviation in this section. As shown in Figure 4.5, there are three curves. The curve *DUT* represents a very small section of the output waveform of the DUT. The *max* and *min* represent the largest and smallest allowed amplitude of the curve. One can see that the amplitude of the curve *DUT* is completely within the allowed range. However, the DUT curve fluctuates more, which can be caused by the distortion of the *DUT.* In this case, the previous algorithm cannot detect the faults in the DUT. That is the reason that we propose in addition a new algorithm by comparing the deviation of the *trend* of a curve. The definition of the angles is shown in Figure 4.6. One can see that (*i-1*), *i* and (*i+1*) are three adjacent points on the output curve of DUT. If one connects two adjacent points *i* and (*i-1*) with a straight line, then an angle $\angle\varphi$ (i-1), between the connected line and x-axis, can be obtained. In this way, with a curve of *N* sampling points, an array of angles $\angle\varphi$ (1), $\angle\varphi$ (2)… $\angle\varphi$ (*i*)…$\angle\varphi$ (*N-1*) can be obtained, which describes the deviation of the trend of a curve.

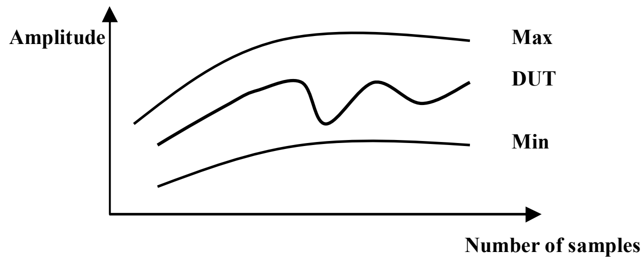

Figure 4.5: A small section of the output curve with fluctuation

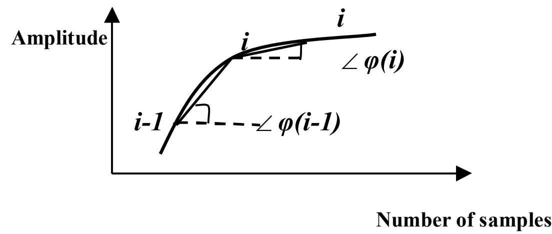

Figure 4.6: The angles on the output curve of the ADC

An overview of the flow of the algorithm in pseudo code is shown in Table 4.2.

Table 4.2: The pseudo code of the flow of the algorithm comparing the deviation by angle (in the time domain)

	Algorithm 1: Deviation comparison by angle
	Initialization
-	Initialize the amplitude array $\angle\varphi$ of each sampling point - Initialize the input stimuli
	Data collection
-	Collect N sampling points instants for the calculation of each DUT
	Main body
1.	Calculate the reconstructed output of the golden devices
2.	Divide reconstructed output into four sections and extract the rising or falling edge
3.	Obtain the acceptable range of the output angle $[\angle\varphi_{min}(i), \angle\varphi_{max}(i)]$
4.	Apply step 1 and 2 to all the other DUTs to obtain $\angle\varphi_{DUT}$
5.	If $\angle\varphi_{DUT}(i) > \angle\varphi_{max}(i)$ obtain $\triangle\angle\varphi(i) = \angle\varphi_{DUT}(i) - \angle\varphi_{max}(i)$ If $\angle\varphi_{DUT}(i) < \angle\varphi_{min}(i)$ obtain $\triangle\angle\varphi(i) = \angle\varphi_{min}(i) - \angle\varphi_{DUT}(i)$ If $\angle\varphi_{min}(i) < \angle\varphi_{DUT}(i) < \angle\varphi_{max}(i)$ define $\triangle\angle\varphi(i) = 0$
6.	Increase the index i, and repeat previous step for best estimate
7.	Calculate the out-of-range ratio by angle $P\angle\varphi$ of each DUT

The initialization and data collection are completely the same as in the previous algorithm. So we will not explain them in detail.

Step 1: Apply the technique of modulo plot [Iro96] to the output of the golden devices.

Step 2: Divide the reconstructed output waveform into 4 sections in the same way as step 2 of the previous algorithm. Similar to the *Am*, an array of angles $\angle\varphi$ can be obtained from each section of the output curve.

Step 3: By comparing $\angle\varphi(i)$ of all the corner cases, the maximum value $\angle\varphi_{max}$ and minimum value $\angle\varphi_{min}$ can be obtained for each element $\angle\varphi(i)$. Parameter i is the ith samples.

Step 4: Apply step 1 and 2 to all DUTs. An array of the angle $\angle\varphi_{DUT}$ of the sampling points from the DUT output can be obtained in the same way as in Step 2.

Step 5: For each element $\angle\varphi_{DUT}(i)$, it is verified whether it is within the range [$\angle\varphi_{min}(i)$, $\angle\varphi_{max}(i)$]. If $\angle\varphi_{DUT}(i) > \angle\varphi_{max}(i)$, the angle deviation $\triangle\angle\varphi(i)$ is defined as:

$$\Delta\angle\varphi(i) = \angle\varphi_{DUT}(i) - \angle\varphi_{\max}(i) \tag{4.4}$$

For the case $\angle\varphi_{DUT}(i) < \angle\varphi_{min}(i)$, we define the angle deviation $\triangle\angle\varphi(i)$ as:

$$\Delta\angle\varphi(i) = \angle\varphi_{\min}(i) - \angle\varphi_{DUT}(i) \tag{4.5}$$

If $\angle\varphi_{DUT}(i)$ is within the range [$\angle\varphi_{min}(i)$, $\angle\varphi_{max}(i)$], the angle deviation is defined as $\triangle\angle\varphi(i)=0$.

Step 6: Finally, the average out-of-range ratio in angle $P\angle\varphi$ of the whole curve is defined as:

$$P\angle\varphi = \frac{\sum_{i=0}^{N}\Delta\angle\varphi(i)}{\sum_{i=0}^{N}\angle\varphi_{\max}(i) - \sum_{i=0}^{N}\angle\varphi_{\min}(i)} \tag{4.6}$$

where N is the total number of sampling points in the rising or falling edge. $P\angle\varphi$ is used to evaluate the faults in the ADC, which will be illustrated later on. The numerator in the formula is the sum of out-of-range parameter $\triangle\angle\varphi$. The denominator is the tolerance of the angles. The ratio between them ($P\angle\varphi$) determines the difference of the trend between the output of the DUT and the golden devices.

4.3.3 Deviation comparison by using the spectrum of the ADC output

The methods in the last two sections (P_am and $P\angle\varphi$) compare the output between the golden devices and the DUTs in the *time* domain. However, as they are all in time domain, the results can be affected by the jitter or time change of the rising and falling edges of the pulse-wave. Therefore, in this section we still carry out the comparison to obtain the signature results, but now in the *frequency* domain. The influence of jitter or time change of the rising and falling edges is less in the latter case. Now, an additional FFT analysis is carried out before proceeding to the comparison steps. The overview flow of the algorithm is shown in Table 4.3.

Table 4.3: The pseudo code of the flow of the algorithm comparing the deviation in the frequency domain

Algorithm 1: Deviation comparison by frequency
Initialization
- Initialize the input stimuli - Initialize the output spectrum
Data collection
- Collect *N* frequency bins for the calculation of each DUT
Main body
1. Obtain the acceptable range of the magnitude of the output spectrum [$F_{min}(i)$, $F_{max}(i)$] from the golden devices. The parameter F(i) represents the magnitude of the ith bin of the output spectrum. 2. Obtain the $F_{DUT}(i)$ of the DUTs 3. If $F_{DUT}(i) > F_{max}(i)$ obtain $\triangle F(i) = F_{DUT}(i) - F_{max}(i)$ If $F_{DUT}(i) < F_{min}(i)$ obtain $\triangle F(i) = F_{min}(i) - F_{DUT}(i)$ If $F_{min}(i) < F_{DUT}(i) < F_{max}(i)$ define $\triangle F(i) = 0$ 4. Increase the index, i, and repeat previous step for best estimate 5. Calculate the out-of-range ratio by frequency P_F of each DUT

The algorithm will now be explained in more detail.

Initialization and data collection: Similar as in the previous algorithms, a collection of golden devices is simulated using a pulse-wave input signal to obtain the fault-free range. However, as shown in Figure 4.7 an additional FFT analysis is required to calculate the output spectrum of all the golden devices. If the total sample points of the output are 4096, the FFT will have an array of 2048 frequency bins. Each frequency bin collects the amplitude from a small frequency range. In Figure 4.7, the $F(i)$ is the ith frequency bin. Similar as in the case of Am, an array of the magnitude of output spectrum F can be obtained for each golden device.

Step 1: By comparing $F(i)$ of all the corner cases, the maximum value $F_{max}(i)$ and minimum value $F_{min}(i)$ can be obtained for each element $F(i)$. Here $F(i)$ denotes the magnitude of the i th frequency bin of the output spectrum.

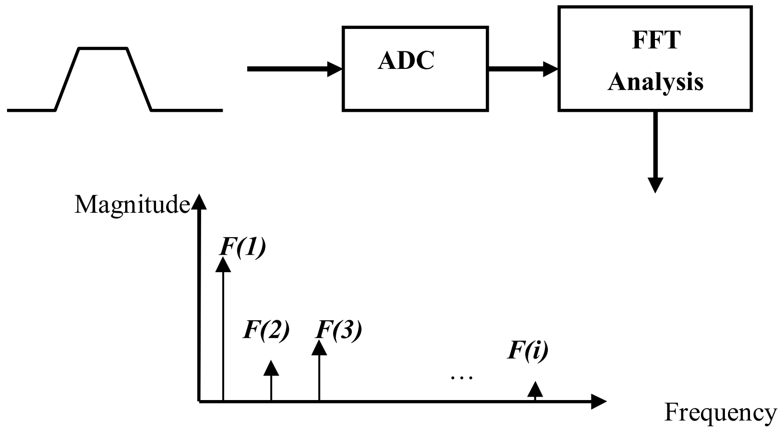

Figure 4.7: Data collection of the array of the magnitude of the output spectrum *F*

Step 2: Apply the pulse-wave input stimulus of the same settings to all the DUTs and calculate the output spectrum. An array of the frequency bins F_{DUT} of the DUT output can be obtained in the same way as in the case of the golden devices.

Step 3: For each element $F_{DUT}(i)$, it is verified whether it is within the range $[F_{min}(i), F_{max}(i)]$. If $F_{DUT}(i) > F_{max}(i)$, the spectrum deviation $\triangle F(i)$ is defined as:

$$\Delta F(i) = F_{DUT}(i) - F_{\max}(i) \tag{4.7}$$

For the case $F_{DUT}(i) < F_{min}(i)$, we define the spectrum deviation $\triangle F(i)$ as:

$$\Delta F(i) = F_{\min}(i) - F_{DUT}(i) \tag{4.8}$$

If $F_{DUT}(i)$ is within the range [$F_{min}(i)$, $F_{max}(i)$], the spectrum deviation $\triangle F(i)$ is defined to be zero.

Step 4: Finally, the average out-of-range ratio in frequency P_F of the whole curve is defined as:

$$P_F = \frac{\sum_{i=0}^{N} \Delta F(i)}{\sum_{i=0}^{N} F_{\max}(i) - \sum_{i=0}^{N} F_{\min}(i)} \tag{4.9}$$

where N is the total number of sampling points. P_F is used to evaluate the performance of the ADCs.

4.4 Simulation results and analysis based on transistor-level design of a 6-bit flash ADC

The transistor-level design of a 6-bit flash ADC is exploited to validate our test methods [Did04]. The ADC is again injected with three different types of faults: offset, gain and bandwidth faults. As the ADC and the fault injection are completely the same as described in section 3.6.1, it will not be explained again.

4.4.1 Simulation of testing a 6-bit flash ADC with offset faults by out-of-range ratio

In practice, the pulse-wave has jitter and variation of the rising or falling edges, which can affect the output results. In order to investigate their influence on the out-of-range ratio, three different types of pulse-waves have been applied to the 6-bit flash ADC respectively. They have a common setup as shown in Table 4.4.

Table 4.4: The simulation setup for *P_am* of the 6-bit flash ADC

Supply voltage	1.2V	Temperature	25 ^oC
Input signal frequency	7MHz	Offset voltage of input signal	0
Number of sampling periods	70	Amplitude	0.46V
Sampling frequency	300MHz	Rise or fall time	10ns

The following cases have been simulated:

1) ***Ideal pulse-wave:*** the setup is as shown in Table 4.4. The ideal pulse-wave still has the slope of rising and falling edges. However, there is a complete absence of noise and jitter.

2) ***Pulse-wave with jitter:*** add a random jitter to the ideal pulse-wave, spectral frequency density=$2.67*10^{-3}$, bandwidth=3.1GHz. The parameter setting of the jitter is the largest acceptable value, which is calculated from the specification of the SNR of the 6-bit ADC [Kob99].

3) ***Pulse-wave with jitter and rise/fall time change:*** set the rise/fall time 0.1 ns different from the pulse-wave with jitter.

After executing the first step of the proposed algorithms, the reconstructed output waveform of a fault-free ADC in a typical case is shown in Figure 4.8. The x-axis shows the reconstructed sample points while the y-axis represents the amplitude of the output. There are 3002 sampling points in total. On either the rising or the falling edge there are around 220 sampling points. As the results of the rising and falling edges are quite similar, only the results of the rising edge are shown.

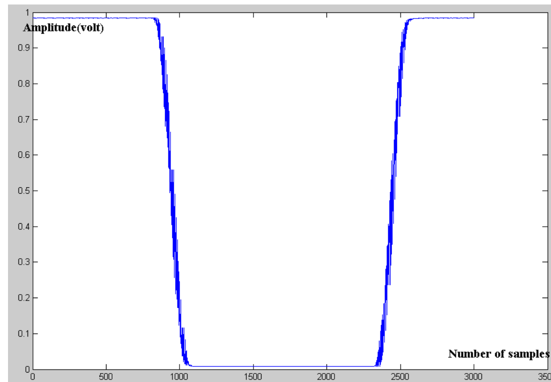

Figure 4.8: The reconstructed output waveform of the fault-free 6-bit flash ADC with pulse-wave input signal

The test algorithms, using amplitude, angle and spectrum to compare the deviation as described in section 4.3, are applied to the 6-bit ADC with injected *offset* faults. The results are shown in Figures 4.9 - 4.11. In the figures, the x-axis shows the ratio of the faulty offset voltage *voffset_fault* with respect to the fault-free offset voltage *voffset* in the typical case. The y-axis of Figures 4.9 – 4.11 denote the values of the *P_am*, $P\angle\varphi$ and *P_F* respectively. The three curves in different markers of each figure represent the results from three different input stimuli (ideal pulse-wave, pulse-wave with jitter, pulse-wave with jitter and rise/fall time change) respectively. The results of the conventional parameters of all the faulty cases have already been shown in Figure 3.7 of Chapter 3. The dynamic performance of the ADC becomes worse if *voffset_fault/voffset* increases. From Figure 4.9, one can observe that if the ratio of *voffset_fault* to *voffset* changes from 9 to 25.6, the *P_am* obtained by the ideal pulse-wave changes from 0 to 0.42. It means that the *P_am* increases as the performance of the ADC becomes worse. One can also observe that the other two curves, obtained from the pulse-wave with jitter and edge variation, have the same trend as the one obtained by the ideal pulse-wave. Hence, it can be concluded that the algorithm by using pulse-wave stimulus can reflect the offset faults of the ADC, even if jitter and edge variations occur. However, these factors change the values of *P_am*.

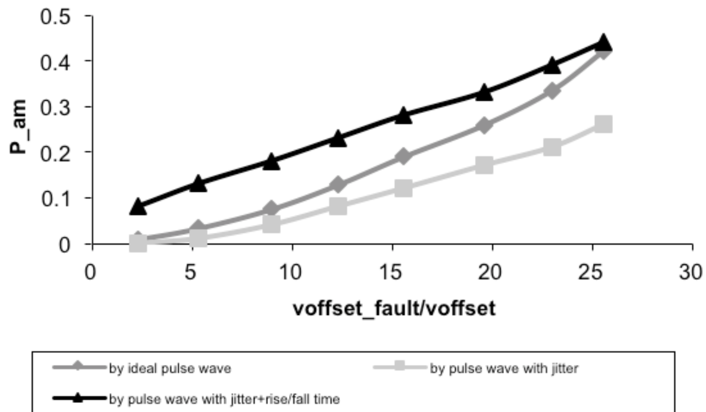

Figure 4.9: The out-of-range in amplitude (*P_am*) of the 6-bit flash ADC with offset fault

The results obtained by the comparison of the angles and spectrum are shown in Figures 4.10 and 4.11 respectively. Both the $P\angle\varphi$ and P_F have the same trend as the P_am. In this case, all these three parameters (P_am, $P\angle\varphi$ and P_F) can reflect the offset faults of the ADC. One can see that the curves in Figures 4.9 – 4.11 are very close to a straight line. If one uses curve fitting of the results to a straight line, the slope of the each curves can be obtained. Compared with the results among them, the slope of the curves of the P_F is the steepest, which is 0.05. Therefore, it is more sensitive to the offset faults as compared to the other two parameters.

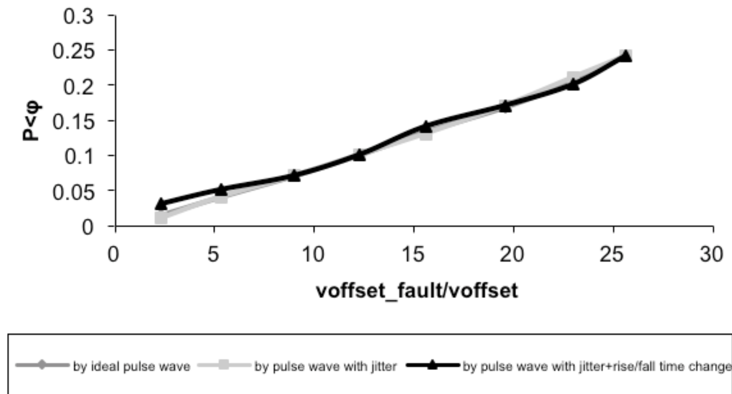

Figure 4.10: The out-of-range in angle ($P\angle\varphi$) of the 6-bit flash ADC with offset fault as parameter

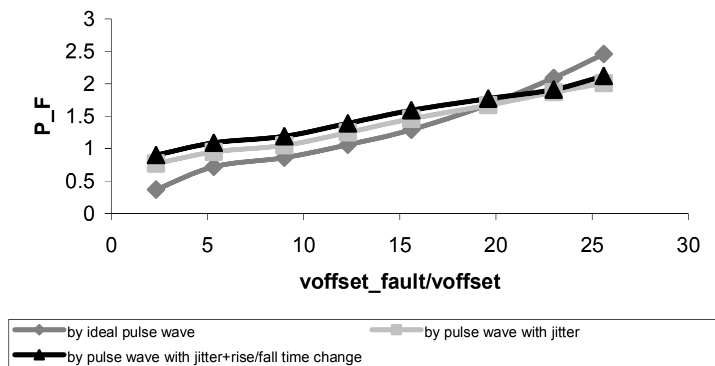

Figure 4.11: The out-of-range in frequency (P_F) of the 6-bit flash ADC as function of the offset fault

The maximum differences between the results tested by the ideal pulse-wave and pulse-wave with jitter and rise/fall time change are 0.25, 0.016 and 0.53 for P_am, $P\angle\varphi$ and P_F respectively. However, the ranges of the deviation of the three parameters are different from each other. For example, with the ideal pulse-wave input stimulus, the P_am increases from 0 to 0.42 as the *voffset_fault/voffset* increases. As a result, the range of the deviation is 0.42. In the same way, with the ideal pulse-wave input stimulus, the ranges of the deviation are 0.23 and 2.1 for the $P\angle\varphi$ and P_F respectively. In this case, P_am is the least robust to

the jitter and edge variation while $P\angle\varphi$ is the most robust.

4.4.2 Simulation of testing of a 6-bit flash ADC with gain faults by the out-of-range ratio

In the case of testing the ADC with gain faults, the test setup is completely the same as the one with offset faults. The results of the three algorithms are shown in Figures 4.12- 4.14. The x-axis denotes the ratio of faulty gain value *gain_fault* to the fault-free gain value *gain* and the y-axis denotes the out-of-range parameters P_am, $P\angle\varphi$ and P_F similar to the previous figures. The curves in different grey graduations are obtained by different types of test stimuli. One can observe that all three parameters have the same trend as the conventional dynamic parameters as shown in Figure 3.6. As consequence, they can reflect the gain fault as well. By comparing the results in Figures 4.12- 4.14, the parameter P_F is the most sensitive to the gain fault as its deviation is maximal with the same type of input stimuli.

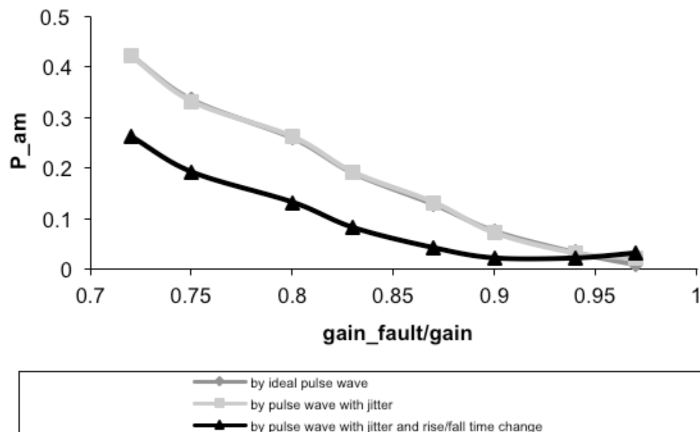

Figure 4.12: The out-of-range in amplitude (*P_am*) of the 6-bit flash ADC with gain fault as variable and stimulus case as parameter

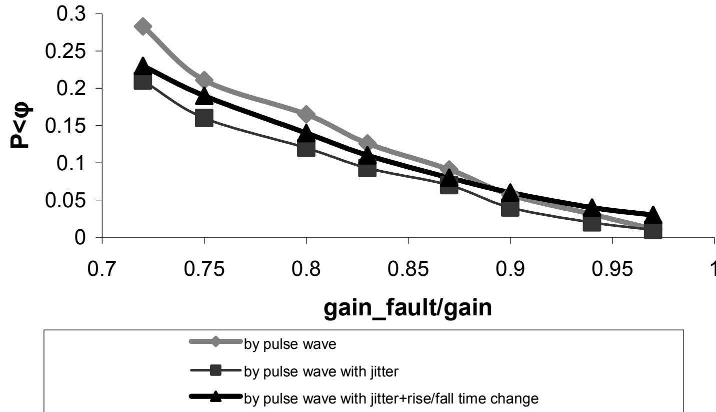

Figure 4.13: The out-of-range in angle ($P\angle\varphi$) of the 6-bit flash ADC as function of the gain fault

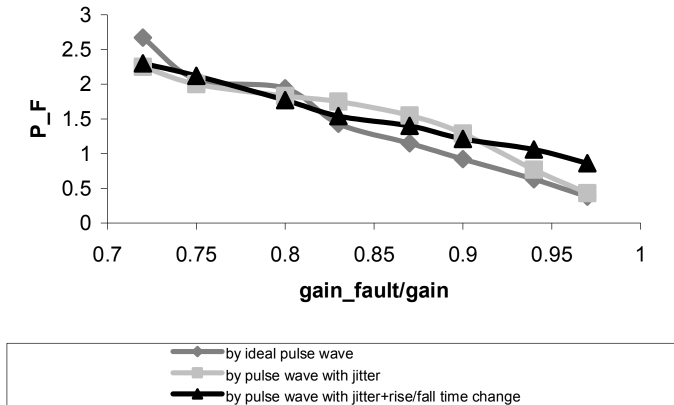

Figure 4.14: The out-of-range in frequency (P_F) of the 6-bit flash ADC as function of the gain fault

There is difference between the results obtained from the ideal pulse-wave and the pulse-wave with jitter and edge variation. The largest difference of the P_am, $P\angle\varphi$ and P_F are 0.16, 0.05 and 0.48 respectively. However, with the ideal pulse-wave stimulus, P_am decreases from 0.42 to 0.01 as the gain fault decreases; $P\angle\varphi$ decreases from 0.28 to 0.01; P_F decreases from 2.46 to 0.37. Compared with their corresponding results deviation by

the ideal pulse-wave input signal, the variation of the $P\angle\varphi$ is relatively small compared to the other two options. Therefore, $P\angle\varphi$ is the most robust to jitter and edge variation.

4.4.3 Simulation of testing a 6-bit flash ADC with bandwidth faults by using the out-of-range ratio

The results of P_am, $P\angle\varphi$ and P_F with regard to bandwidth parametric faults are shown in Figures 4.15 – 4.17. The x-axis is the ratio of the faulty bandwidth BW_fault to the fault-free bandwidth BW, while the y-axis shows the values of the out-of-range ratio by amplitude, angle or spectrum. From the figures we observe that the trends of the results of P_am and $P\angle\varphi$ match the trends of the conventional test results shown in Figure 3.8. It means that the P_am and $P\angle\varphi$ can detect the bandwidth faults of a 6-bit flash ADC. In Figure 4.17, irrespective which type of the pulse-wave, the trend of P_F can not match the trend of conventional test results very well. For example, the P_F obtained from the ideal pulse-wave decreases as the BW_fault/BW increases from 0.052 to 0.077, which means the P_F can detect the bandwidth faults. However, as BW_fault/BW decreases from 0.52 to 0.038, the P_F decreases while it should increase if correct. If one observes the P_F obtained from the other two types of pulse-waves, it does not always show a correct trend either. As a result, the P_F is not a robust parameter to detect the bandwidth fault of the 6-bit flash ADC.

In case the ideal pulse-wave is the input signal, the variation in the P_am and $P\angle\varphi$ as function of the bandwidth faults are 1.5 and 1 respectively. The largest difference between P_am obtained from the ideal pulse-wave and P_am obtained from the pulse-wave with jitter and edge variation is 0.26. For $P\angle\varphi$, the largest difference is 0.05. In this case, $P\angle\varphi$ is less affected by the jitter and edge variation.

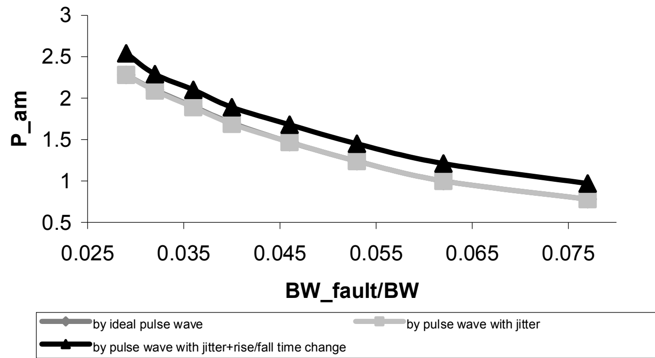

Figure 4.15: The out-of-range in amplitude (*P_am*) of the 6-bit flash ADC with bandwidth fault

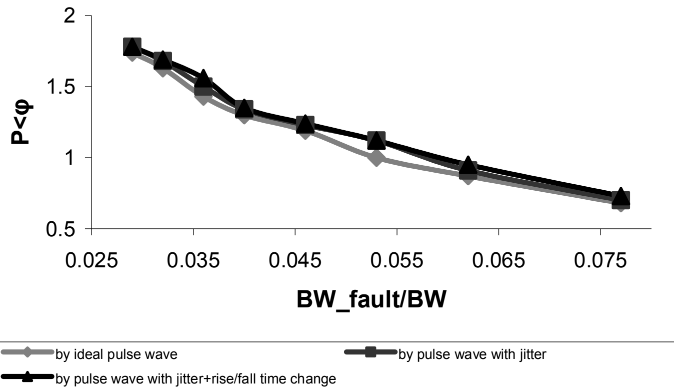

Figure 4.16: The out-of-range in angle ($P\angle\varphi$) of the 6-bit flash ADC with bandwidth fault

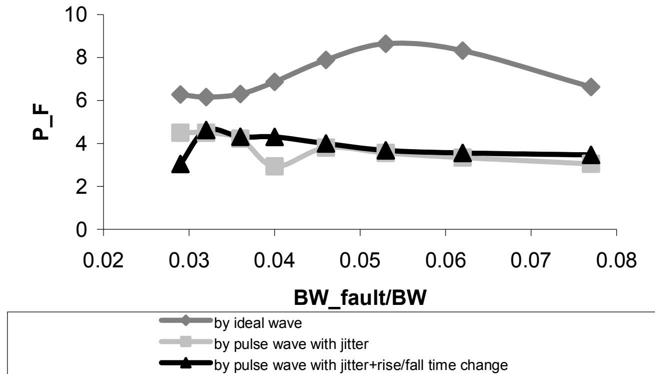

Figure 4.17: The out-of-range in frequency domain (*P_F*) of the 6-bit flash ADC with bandwidth fault

From the results shown in sections 4.4.1 – 4.4.3, the features of the out-of-range parameters (*P_am*, $P\angle\varphi$ and *P_F*) for testing 6-bit flash ADC are summarized in Table 4.5. In the table, the *D* represents that the fault is detectable via the corresponding out-of-range parameter; the *S* denotes the parameter being the most sensitive to the faults compared with the other two; the *R* represents the parameter which is the most robust to jitter and the edge variation of the pulse-wave stimulus. From Table 4.5, it can be seen that the *P_F* is the most sensitive to the offset and gain faults. However, it cannot detect bandwidth faults. The *P_am* and $P\angle\varphi$ can detect all three types of faults. In the case there is jitter and edge variation, the $P\angle\varphi$ is the most robust as compared to the other two parameters.

Table 4.5: The properties of the out-of-range parameters (*P_am*, $P\angle\varphi$ and *P_F*) for testing a 6-bit flash ADC

	Offset faults	Gain faults	Bandwidth faults
P_am	D	D	D
$P\angle\varphi$	D & R	D & R	D & R
P_F	D & S	D & S	-

4.5 Simulation results and analysis based on a Labview model of a 12-bit pipelined ADC

As the 6-bit flash ADC has no matching silicon implementation, a 12-bit pipelined ADC has been exploited to validate the proposed algorithms [Gee06]. For simulation, the 12-bit pipelined is modeled at system-level via Labview. As the structure of the 12-bit pipelined ADC has already been explained in Chapter 1, it will not be explained anymore in this chapter. The settings of the input pulse-wave stimuli are shown in Table 4.6. The rising and falling edges of the pulse-wave are modeled with 7-bit linearity as suggested in [Jin05]:

$$x(t) = v_{os} + \eta[t + 0.04*(t^2 - t)] + n(t) \tag{4.10}$$

where *x(t)* represents the amplitude of the slope of the pulse-wave, v_{os} denotes the offset voltage, η is the slope and *n(t)* represents the noise. The part 0.04*(t^2-t) corresponds to the 7-bit nonlinearity property of the edges. For the entire pulse-wave, a Gaussian white noise of 3 LSB standard deviation has been added to the amplitude of the pulse-wave.

As explained in section 3.7.1, only the gain fault of the amplifier in the sub-stage is injected into the Labview model of the ADC, since only the gain fault is related to the way of fault emulation in the measurements. This has already been explained in section 3.7.1, and hence we will not give more explanation in this chapter.

Table 4.6: The settings of the pulse-wave stimuli in the Labview simulation of a 12-bit pipelined ADC

	Input frequency (*MHz*)	Duty cycle (%)	Rise or fall time (*ns*)	Number of samples
Pulse 1	1.8	50	100	4096
Pulse 2	1.8	50	100	16384

The simulation results of *P_am*, $P\angle\varphi$ and *P_F* are shown in Figures 4.18 – 4.20 respectively. In these figures, the x-axis denotes the values of the gain of each sub-stage of

the ADC and the y-axis denotes the results of the out-of-range ratio in amplitude, angle or spectrum. One can observe that as the gain decreases from 64dB to 42.5dB, the values of the *P_am* and *P_F* obviously increase. If the gain is 60dB, 62.5dB or 65dB, the ADC is taken as the golden device. The conventional dynamic parameters (THD, SNR and SINAD) versus the gain have already been shown in Figure 3.23, which indicates that the decrease of the gain will degrade the dynamic performance of the ADC. In this case, the values of the out-of-range ratio should increase. Obviously, the trends of *P_am* and *P_F* are in agreement with this. However, the trend of the curve of the parameter $P\angle\varphi$ cannot match the one of the dynamic parameters in the case the gain changes from 57.5dB to 42.5dB. Hence, the algorithm of the comparison of angles cannot reflect the faults in the 12-bit pipelined ADC. The proposed test method is supposed to distinguish the faulty devices from the fault-free devices. As a result, Figures 4.18 - 4.20 also include two fault-free ADCs in which the gains are 61dB and 64dB. For $P\angle\varphi$, the values of the two fault-free devices are equal or even larger than the ones of the faulty devices. Therefore, it cannot classify the faulty and fault-free devices. For *P_am* and *P_F*, the values of the faulty-free devices are smaller than the faulty devices. As a result, the faulty and fault-free devices can be classified by *P_am* and *P_F*.

Two different types of pulse-waves have been applied as test stimuli. The only difference between them is the number of samples. For the out-of-range parameter *P_am*, the deviation of the results obtained by *pulse* 2 is larger than the one obtained by *pulse* 1. For the metric *P_F*, it is the same. An increased deviation means more sensitivity of the parameters with respect to the faults. As a result, the input stimulus *pulse* 2, which has more samples of the input pulse-wave signal, will result in a better fault detection of the *P_am* and *P_F*. One can also observe that the slope of the results of the *P_F* is steeper, which means it is more sensitive to gain faults in the 12-bit pipelined ADC.

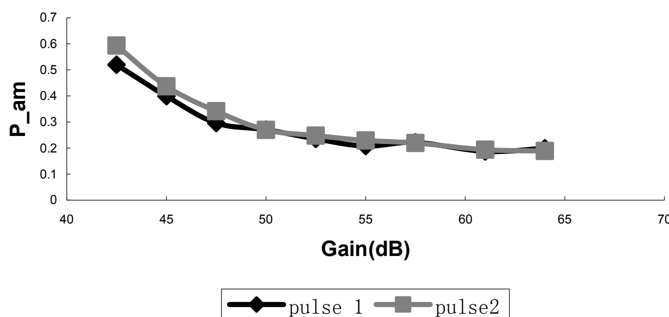

Figure 4.18: The P_am of the 12-bit pipelined ADC in the Labview model with the gain as variable and two pulses as parameter

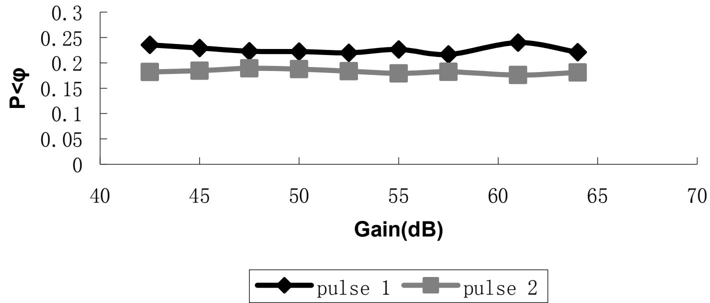

Figure 4.19: The *P∠φ* of the 12-bit pipelined ADC in the Labview model with the gain as variable and two pulses as parameter

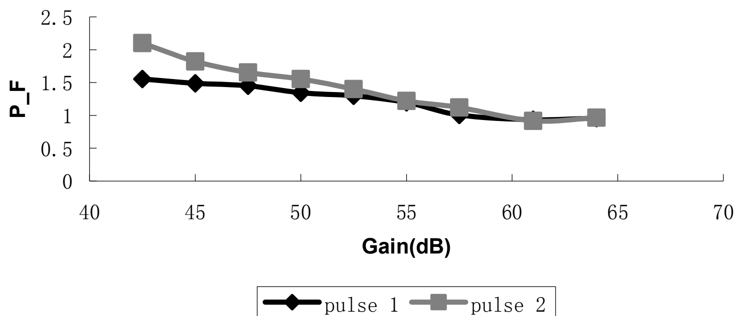

Figure 4.20: The *P_F* of the 12-bit pipelined ADC in the Labview model with the gain as variable and two pulses as parameter

4.6 Measurement setup and results of the 12-bit pipelined ADC

For validating our algorithms, a 12-bit pipelined ADC in the Aqua chip has been selected as target device, which is the same device used in the measurements of Chapter 3. As explained in Chapter 3, either the supply voltage of the Labview model or the gain of the substage of the ADCs in the measurement set-up cannot be changed. It is also very difficult to accurately estimate the relation between the gain and the supply voltage of the 12-bit pipelined ADC. In this case, the faulty DUTs are again emulated by changing the

supply-voltage level, which is not the same as the simulation. One fault-free DUT is also included in the measurement, which is the ADC operating at 1.2V. Figure 3.28 shows the conventional dynamic parameters with different voltage levels. The dynamic performance degrades in case the supply voltage decreases. In order to investigate the robustness of the method, four different pulse-waves have been applied to the device respectively; they have different rise and fall times and a different number of samples have been used. The parameters of the settings of these pulse-waves are listed in Table 4.7. To emulate the collection of golden devices, the ADC operating at the voltage levels equal to 1.1V or 1.3V have been used as golden devices.

As the input pulse wave ideally always starts from the rising edge in the simulation, the starting sampling point of the rising edge at the output of the ADC is always the first sampling point of the pulse wave. However, in the *measurements*, the input pulse wave cannot always start from the same position every time, as it is limited by the measurement setup. The sampling point of the rising edge at the ADC output is hard to decide on. In our case, the starting of the rising edge is the sampling point on the rising edge, which firstly reaches 10% of the input pulse wave amplitude, since normally the rising/falling edge is defined starting from 10% of the amplitude. Here one should be very careful that the selection of the starting sampling point for both golden devices as well as the DUTs should have the same criterion, for example both 10% of the pulse wave amplitude; this is because the basic principle of the method is comparison of the similarity. Otherwise, it can result in completely wrong measurement results and cause errors in the fault classifications.

Table 4.7: The settings of the pulse-wave stimuli in the measurement of the 12-bit pipelined ADC

	Input frequency (*MHz*)	**Duty cycle (%)**	**Rise or fall time (*ns*)**	**Number of samples**
Pulse 1	1.8	50	100	4096
Pulse 2	1.8	50	100	16384
Pulse 3	1.8	50	200	16384
Pulse 4	1.8	50	200	32768

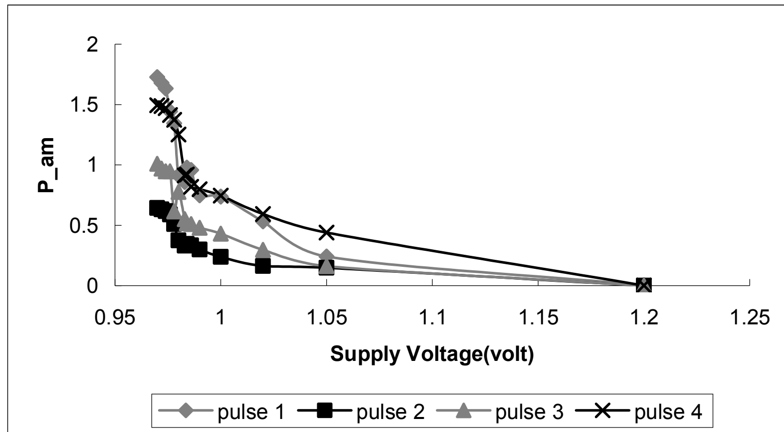

Figure 4.21: The measurement results of *P_am* of a 12-bit pipelined ADC with the supply voltage as variable

Comparing Figure 4.21 with Figure 3.28, the *P_am* shows a similar trend as the dynamic specifications with the variation of the supply voltage. One can observe if the supply voltage drops below 1.1 V, the values of the *P_am* become increasingly larger. However, if it drops around 1.0 V, the slope of the curve suddenly becomes steeper. From section 3.8.2, one knows that if the ADC is operating at a voltage below 1.1V, it is defined as a faulty device by using the conventional test method. As a result, *P_am* is as sensitive as the conventional dynamic parameters in detecting faults of the ADC. In Figure 4.21, there is also the value of the *P_am* in the case the ADC is operating at 1.2V. In this case, the ADC is defined as being fault-free. Obviously, the *P_am* of the fault-free ADC is almost zero, smaller than the faulty devices. The difference of the *P_am* between the faulty and fault-free devices is at least 0.28, 0.15, 0.16 and 0.44 for pulse 1, pulse 2, pulse 3 and pulse 4 respectively. Therefore, the *P_am* can distinguish the faulty devices from the fault-free devices.

Comparing the curves of the *P_am* obtained with different pulse-wave input stimuli in Figure 4.21, their trends are similar. The values of *P_am* do not change too much either if the number of sampling points increase from 4096 to 32768, or in the case the rise and fall times are doubled. This means that the parameter *P_am* is very robust with regard to the rise and fall times of the edges and the number of samples of the pulse-wave input stimuli.

The measurement results of the out-of-range metric $P\angle\varphi$ are shown in Figure 4.22. The trend of the curves is not similar to the one of the conventional dynamic parameters. Therefore, one can conclude that the $P\angle\varphi$ cannot detect the faults in dynamic parameters in the 12-bit pipelined ADC.

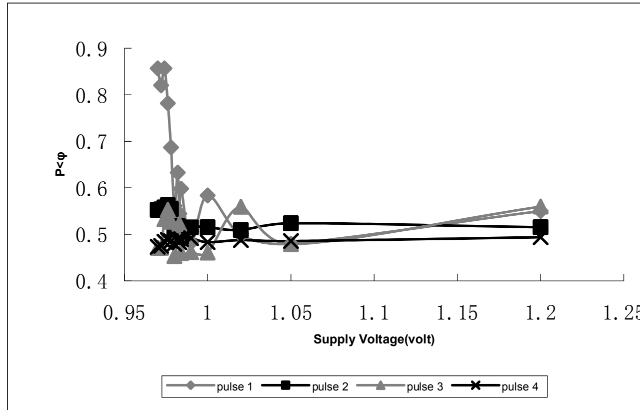

Figure 4.22: The measurement results of $P\angle\varphi$ of a 12-bit pipelined ADC with the supply voltage as variable

Figure 4.23 shows the results of the metric *P_F*. If the supply voltage operates from 0.98V to 1.2V, the curves are relatively flat. However, if one compares the value of the *P_F* between the ADCs with 1.2 V and 1.05V, the difference is at least 0.91 for pulse 2, pulse 3 and pulse 4. For pulse 1, the difference between the fault-free and faulty devices becomes obvious only if the supply voltage decreases to 1V. In case it is below 0.98V, the *P_F* increases much more. The whole trend of the curves is similar to the one of the conventional dynamic parameters shown in Figure 3.28. Therefore, the *P_F* can decide if the dynamic parameters of the ADC are faulty or fault-free. However, it is much more sensitive to the faults than the *P_am*, as the slope of the curves obtained by *P_F* is much steeper. If one observes the curves of the *P_F* obtained by different stimuli, the one obtained by *pulse* 4 has the steepest slope and the one obtained by *pulse*1 has the flattest slope. While comparing the pulse-wave input stimuli with four different settings, one can observe that the major difference is that the number of samples of the rising and falling edges is larger. Hence, for the *P_F*, if the number of samples of the edge increases the results change more significantly if the supply voltage is below 0.98V.

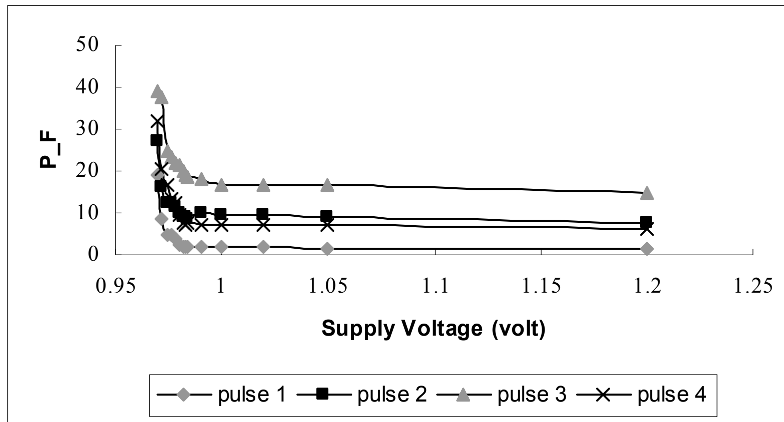

Figure 4.23: The measurement results of *P_F* of a 12-bit pipelined ADC with the supply voltage as variable

The simulation and measurement results of the metrics *P_am*, $P\angle\varphi$ and *P_F* of the 12-bit pipelined ADC are summarized in Table 4.8. In the Table, *D* represents the corresponding parameter can detect the faults; *S* means the parameter is more sensitive to the faults than the other two parameters. Both simulation and measurement results indicate that *P_am* and *P_F* can reflect the faults in the pipelined ADC while $P\angle\varphi$ can not. Compared with *P_am, P_F* is more sensitive to the faults.

Table 4.8: Features of the out-of-range parameters in detecting the faults of a 12-bit pipelined ADC

	P_am	$P\angle\varphi$	***P_F***
Simulations	D	-	D & S
Measurements	D	-	D & S

4.7 Impact of the position of the starting sampling points on measurement results

From sections 4.3.1 and 4.3.2, we know that the rising edge is used to calculate P_am and $P\angle\varphi$. It will be of interest to know the impact of the position of the rising edge. First, it was attempted to derive a mathematical expression to investigate this issue. However, in the

equations 4.3 and 4.6, *P_am* and $P\angle\varphi$ and are calculated by the accumulation of the results from each sampling point. In this case, it is impossible to use a mathematical method; however several experiments using the measurement data have been carried out for the investigation. In the measurements, four pulse waves with different number of sampling points or the rising/falling times have been exploited as the test stimuli. In order to simplify the experiments, only the measurement data from pulse 1 and pulse 4 have been used in this section, since they have the largest deviation, both in different number of sampling points and rising /falling time.

4.7.1 The impact of the starting sampling point on *P_am*

The positions of the starting sampling point of all the devices are changed at the same time, including golden devices (with supply voltages 1.1V and 1.3V) and also the DUTs (with supply voltages 1.2V, 1.05V, 1.02V…0.97V). In Figure 4.21, the starting rising edge is defined as the sampling point first reaching 10% of the amplitude of the input pulse wave; this because the rising/falling edges are normally defined as 10% to 90% of the amplitude. In this section, also the starting sampling points with 5% and 20% of the amplitude have been included. Figure 4.24 shows the results of *P_am* in the case of the input pulse wave 1. The x-axis denotes the supply voltage of the ADC and y-axis denotes the value of *P_am*. There are 3 curves in Figure 4.24, which represent the results of different starting sampling points (5%, 10% and 20% of the amplitude of the pulse wave) respectively. The trends of all the three curves show that as the supply voltage decreases, *P_am* becomes larger. For the two curves with starting sampling points of 5% and 20% amplitude, the *P_am* of the faulty devices (from 0.97V to 1.05V) are still obviously larger than the fault-free device (1.2V). As a result, it can distinguish the faulty devices from the fault-free devices. Figure 4.25 shows the *P_am* results in the case of input pulse wave 4. The x-axis and y-axis are the same as Figure 4.24. The three curves are also obtained by different starting sampling points (5%, 10% and 20%). Similar to the results of pulse 1, the two curves in the cases of 5% and 20% can still distinguish the faulty devices as in the case of the curve with 10%.

Since the settings of pulse 2 and 3 are within the deviations of pulse 1 and pulse 4, they should also provide similar results as pulse 1 and 4. In conclusion, if the starting sampling point changes from 5% to 20% of the amplitude for both golden devices and DUTs, the *P_am* can still distinguish faulty devices from the fault-free devices.

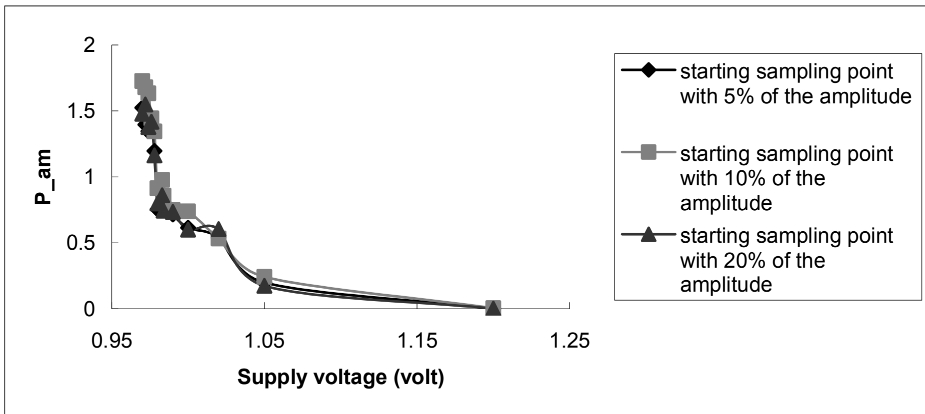

Figure 4.24 *P_am* with different starting sampling points in the case of input pulse 1

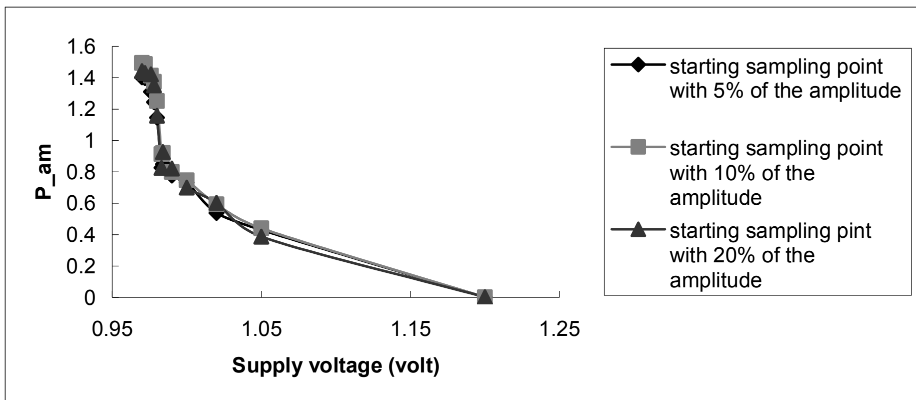

Figure 4.25 *P_am* with different starting sampling points in the case of input pulse 4

4.7.2 The impact of the starting sampling point on *P<φ*

From the measurement results shown in Figure 4.22, it was concluded that *P<φ* cannot reflect the faults in dynamic parameters in the 12-bit ADC. However, it is still of interest to know if the position of the starting sampling point can affect the results of *P<φ*. In this case, the same experiments on *P_am* have also been carried out on *P<φ*. The results are shown in Figures 4.26 and 4.27. The x-axis is the supply voltage of the device while the y-axis is the value of *P<φ*. The three curves are the results in the case of different starting sampling points,

which are 5%, 10% and 20% of the pulse wave amplitude respectively. One can see that in Figure 4.26, the trend of the three curves is similar as the conventional dynamic parameters in Figure 3.28. However, if the supply voltage is larger than 0.983V, the *P*<*φ* of the faulty devices is either larger or very close to the ones of the fault-free devices. Hence it cannot distinguish the faulty devices from the fault-free devices. If the voltage is smaller than 0.983, *P*<*φ* has some bumps in the curve, which cannot reflect the faults in the devices very well. The curves in Figure 4.27 have a different trend with respect to each other. However, while looking at the scale of *P*<*φ*, it only ranges from 0.47 to 0.54. The curves are all very flat. The trends of the curves are also very different from the conventional dynamic parameters. In conclusion, even if the position of the starting sampling points for *P*<*φ* are changed, it still cannot reflect the dynamic faults of the 12-bit pipelined ADC.

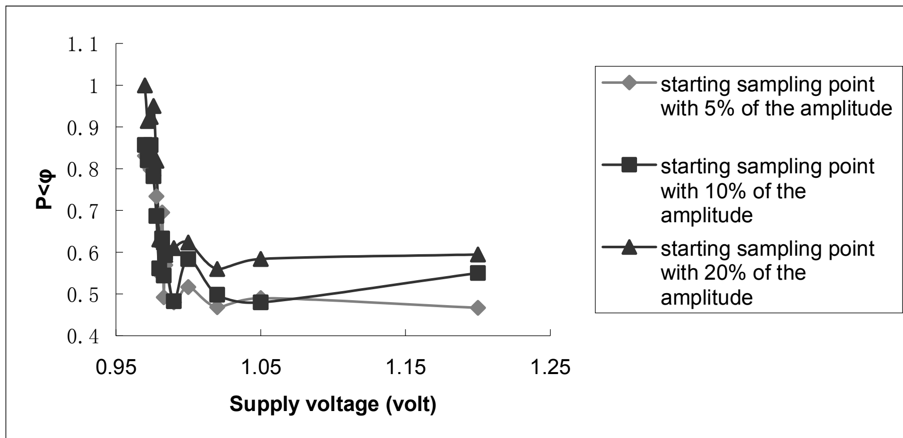

Figure 4.26 P<*φ* with different starting sampling points while applying input pulse 1

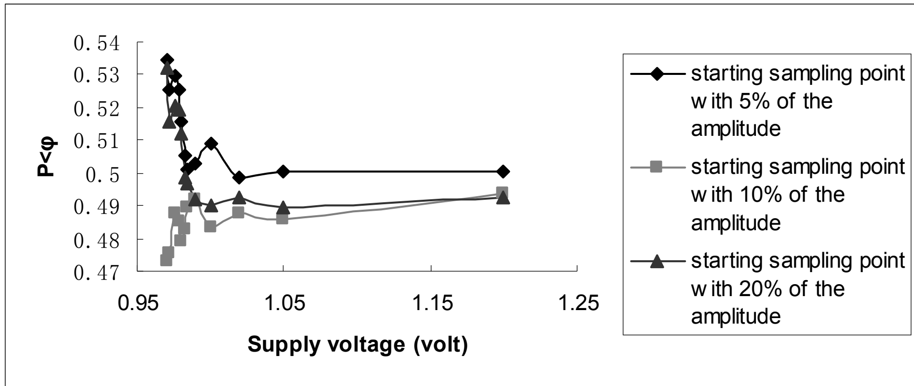

Figure 4.27 ***P<φ*** **with different starting sampling points as result of input pulse 4**

4.8 Comparison between the proposed algorithms and the conventional dynamic test method

In this section, we will compare the proposed algorithms with the conventional dynamic test method for several important aspects of production testing, like test stimulus, output data post-processing, test results, test time and quality of classification.

1) Input Test Stimulus

In the conventional specification testing of an ADC, a high quality analogue ramp or sine-wave signal is required, which is expensive to generate either on-chip or off-chip for a multi-site test environment. However, in the proposed testing method, an adapted pulse-wave, which is relatively easy to generate in a platform-based design, is exploited as the test stimulus. Obviously, in case an ADC is integrated into a platform-based design, the proposed method is less expensive and simpler for a multi-site test of the ADC.

2) ADC Output Data Post-processing

The FFT analysis and histogram method are usually applied to calculate the dynamic and static parameters respectively in the specification test. They are complicated and time consuming. However, for obtaining the P_am and $P\angle\varphi$, only a simple calculation based on the time domain output results has to be carried out. If one carries out the Matlab programs of the FFT analysis and the proposed algorithms on the same computer, the time of computation

is 0.076s and 0.01s respectively. This means a reduction of 87%. As a result, it can save more time and data processing power.

3) Test Results

The accurate specification results of parameters can be determined by using the conventional ADC test methods. The proposed method can only obtain a signature result to distinguish faulty devices from the fault-free devices. However, as discussed before, it is proposed as a quick and simple pre-test suitable for implementing in a multi-site environment. After this pre-test, the failed devices are discarded and only the devices which pass the pre-test, have to undergo the complicated and time-costly specification test. If the yield of the chips is within certain values, it can reduce the production test time and costs significantly.

4) Test Time

We define the total test time of the conventional ADC test to be:

$$T_c = t_{s_c} * \frac{N_{DUT}}{s_c} \tag{4.11}$$

where t_{s_c} denotes the test time for a conventional test for testing s_c sites, while N_{DUT} denotes the total number of DUTs. In this analysis, it is assumed the pre-test perfectly detects the faulty devices without any misclassification. The total test time of the ADC test with the proposed pre-test can be defined as:

$$T_n = t_{s_p} * \frac{N_{DUT}}{s_p} + t_{s_c} * \left(\frac{N_{fault-free}}{s_c} \right) \tag{4.12}$$

where t_{s_p} denotes the time of pre-test for testing s_p sites, $N_{fault\text{-}free}$ denotes the number of DUTs passed after the pre-test. The yield can be defined as:

$$yield = \frac{N_{fault-free}}{N_{DUT}} \tag{4.13}$$

The ratio between the total test time with and without pre-test can be calculated as:

$$\frac{T_n}{T_c} = \frac{t_{s_p}}{t_{s_c}} * \frac{s_c}{s_p} + yield \tag{4.14}$$

If one assumes t_{s_p} / t_{s_c} = 0.01/0.076 while using the P_am or $P\angle\varphi$ for the pre-test, the relationship between the T_n/T_c and *yield* is shown in Figure 4.28. The x-axis denotes the yield while the y-axis denotes T_n/T_c. One can observe that the proposed method can increasingly

reduce the production test time as the yield becomes lower. If $\frac{s_c}{s_p}$ is 1, 0.5 or 0.01, the proposed method can save test time only if the yield is less than 87%, 93% or 99.8% respectively.

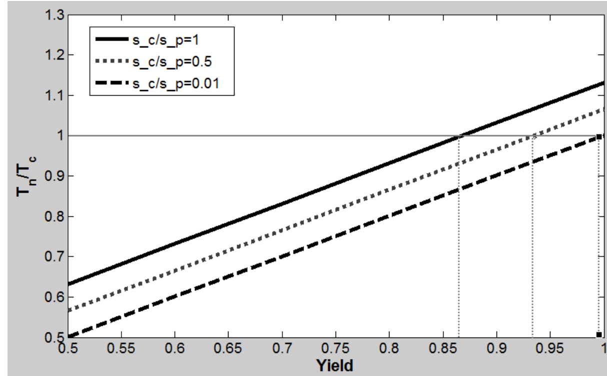

Figure 4.28: The ratio T_n/T_c vs. yield using the *P_am* or *P∠φ* for the pre-test with the ratio of sites as parameter

While using the *P_F* for the pre-test, the FFT analysis is also required like in the conventional test method. In this case, the ratio $t_{s_p}/t_{s_c} \approx 1$. The ratio T_n/T_c versus the *yield* is shown in Figure 4.29. Compared with the results in Figure 4.28, obviously with the same *yield* and *s_c /s_p* the pre-test using *P_F* can not reduce the test time as much as the one using the *P_am*. If *s_c /s_p* is about 1, the proposed method can also not save test time with parameter *P_F*. On the other hand, if the ratio *s_c /s_p* is 0.5 or 0.01, the proposed method can save test time only if the yield is less than 50% or 99% respectively. As a result, there is no benefit of the method in the case of a matured process.

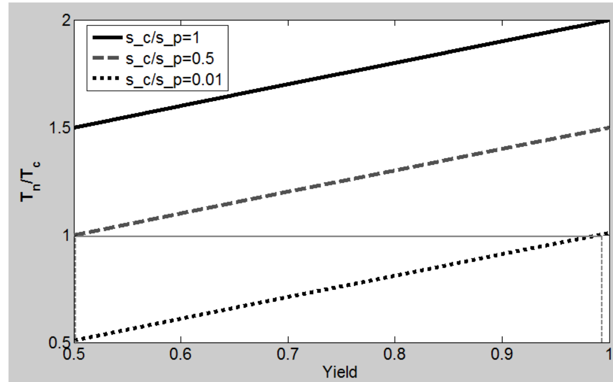

Figure 4.29: The ratio T_n/T_c vs. yield using the *P_F* for the pre-test

5) Quality of classification

Assume that the conventional dynamic test is the one that measures the parameter P, and one defines that an ADC which satisfies P<s can pass the conventional test, where s is the upper limit of P. If the pre-test is the measurement of parameter T, and one assumes an ADC can pass the pre-test with T<t, where t is the upper limit of T. Then the yield loss Y_L can be defined probabilistically as [Str10]:

$$Y_L = Pr\ (P<s|T>=t) \quad (4.15)$$

It means that the devices, which can pass the conventional dynamic test but fail at the pre-test, are categorized to the yield loss.

The test escape T_E can be defined probabilistically [Str10]:

$$T_E = Pr\ (P>=s|T<t) \quad (4.16)$$

Therefore, the devices, which can pass the pre-test but fail at the conventional dynamic test, are accounted for the test escape.

In Figure 3.28, one can observe that the conventional dynamic test rejects 9 faulty devices. For our proposed methods, the devices are defined as faulty devices if the out-of-range parameters are larger than the one of the fault-free device with supply voltage 1.2V. In Figures 4.21 - 4.23, one can observe that a maximum of 11 devices are distinguished as faulty devices by the proposed pre-test parameter *P_am*. According to the results in Figure 4.21 - 4.23, there are 2 devices which are misclassified by the proposed pre-test, which will lead to yield loss according to Equations 4.15 and 4.16. As the number of devices is very limited, we

cannot quantify the number of the misclassifications. However, one can still conclude that there are misclassifications in the proposed test method.

4.9 Conclusions

In this chapter, an ADC pre-test based on three novel algorithms has been proposed. In these three algorithms, a simple digital wave form, an adapted pulse-wave, is taken as the test stimulus as it is suitable to be generated in a platform-based design, in which more and more ADCs are integrated nowadays. Using a simple and fast data processing of the algorithms, a signature results, the out-of-range ratio in amplitude, angle or frequency (P_am, $P\angle\varphi$, P_F), can be obtained to decide if the DUTs pass or fail the pre-test. The basic concept of these three algorithms is evaluating the faults in the ADCs by comparing the similarity between the outputs of golden devices and DUTs in the time or frequency domain.

The transistor-level design of a 6-bit flash ADC has been used to verify the algorithms. Three typical faults in a flash ADC (gain, offset and bandwidth faults) have been injected into the first stage amplifier to emulate the faulty devices. The simulation results show that the P_am and $P\angle\varphi$ can detect all types of faults. However, the P_F can only detect the offset and gain faults. The $P\angle\varphi$ is the most robust to the jitter and rise-and-fall-times variation of the input pulse-wave stimulus.

Both the simulations and measurements of a 12-bit pipelined ADC have been exploited to validate the algorithms as well. Both the simulation and measurement results show that the P_am and P_F can reflect the faults in the ADC while $P\angle\varphi$ cannot. The more samples of the rising and falling edges of the pulse-wave input signal, the more sensitive P_F is to the faults in the ADC as was to be expected. However, the P_am is more robust to the number of samples of the edges as shown in the measurement results. In this case, less samples of the input stimulus are required and the test time can be reduced.

For the measurement results, the investigation on the impact of the starting sampling point position has been carried out on P_am and $P<\varphi$. The results show that if the starting sampling point changes from 5% to 20% of the pulse wave amplitude for both golden devices and DUTs, P_am can still distinguish the faulty devices while $P<\varphi$ still cannot.

From both the results of the 6-bit flash ADC and 12-bit pipelined ADC, one can observe that P_am is the most stable metric, which can detect faults in the ADC. However, the $P\angle\varphi$ and P_F have limitations with respect to the types of faults or the ADC architecture. As result,

the *P_am* can be a more widely used parameter for detecting faults of the ADC.

For the proposed test method, the input test signal can be generated on-chip and the algorithms are very suitable for on-chip calculation in a multi-site test environment. Based on this precondition, we proposed to exploit it as a pre-test to filter out most of the faulty devices. The complicated and time-consuming specification test is only necessary for the remaining devices. In this way, it will help to reduce the production test time and cost of ADCs significantly, especially if the devices are fabricated in a not fully matured process.

In the method of using amplitude to detect the ADC faults, the rising edge is used to calculate the results. The selection of the starting sampling points of the rising edge has been done manually in this thesis. In the future, for better repeatability of the test results, a software program should be developed to do the selection. In the pre-test, also misclassification might exist as happening in all test methods. However, as currently the number of devices is limited, the misclassification of the proposed test method has to be investigated in the future.

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Chapter 5

Predicting ADC Specifications with a Low-Quality Digital Signal

5.1 Abstract

In this chapter, a new method is presented to test dynamic and static parameters of an ADC. A noisy and nonlinear pulse is applied as test stimulus, which can be easily generated in a multi-site test environment. The conventional test parameters are predicted using a machine-learning-based approach. A training step is required in order to build a so-called mapping function using alternate signatures and the conventional test parameters; these are all measured from a set of data converters. As a result, in the case of industrial testing, only a simple signature-based test is performed on the Devices-Under-Test (DUT). The signature measurement results are input to the mapping function that is used to predict the conventional dynamic and static parameters.

5.2 Introduction

Recently, much research on machine-learning-based testing for RF or mixed-signal circuits has been carried out. In [Goy05], a high-speed ADC is tested on a low cost mixed-signal tester. Generating a pure and high frequency sine wave for the dynamic testing of a high-speed ADC is very expensive in a production-test environment. In order to overcome this difficulty, one generates a high-frequency data source by mixing two low-frequency signals. Band-pass filters are applied to extract the desired signal, of which the frequency is the sum of the two low frequencies. However, the quality of the extracted signal is not sufficient to obtain the dynamic parameters accurately. In the approach, an unconventional test method is proposed. A prediction function is generated using multivariate adaptive regression splines (MARS) [Fri91] and the data of training devices. Finally, by using the prediction function, the values of the dynamic parameters can be predicted from the signature results. There are still some differences between the predicted results and the conventional test results. However, this is less than 1dB, which is acceptable in most production environments.

The work in [Kim07] is focused on the loop-back test of the ADC and a Digital-to-Analogue Converter (DAC). The signature results are used to predict the dynamic parameters of both the ADC and DAC in a loop-back test. The MARS algorithm is exploited to generate a mapping function similar as used in [Goy05]. Using the mapping function, indicating the relationships of the outputs between the ADC, the DAC and the loop channel, the inherent fault-masking problem of the loop-back test can be solved. This approach is very interesting because it avoids the requirement of an external high-cost analogue signal generator. But considering only the test of an ADC there is a compulsory requirement for a DAC and additional circuitry to realize an analogue signature generator between the two converters.

The authors in [Han05] propose a low-cost built-in test for RF circuits by using an envelope detector. Compared with the nominal frequency of RF circuits, a relatively low-frequency two-tone signal is applied as test stimulus. The envelope of the output is obtained by an on-chip envelope detector. Subsequently, wavelet transforms are carried out on the output of the envelope detector. In this case, the wavelet coefficients of the RF circuits can be obtained. They are then mapped to the specification space of the DUT by the mapping function. This solution is also interesting considering that it is used to test RF components, which are the most expensive analogue components to test. However, similar to the previous

solution, there is the requirement of additional circuitry (envelope detector) to generate the signature.

Considering the previously cited test methods, we propose a similar machine-learning-based approach, using an alternate signature to predict conventional test parameters. But for our solution, we minimize the need of additional circuitry to generate the stimulus and to capture signatures. In Chapter 4, it has been proven that the out-of-range percentage (*ORP*) in amplitude is a robust signature result to filter out most of the faulty devices. Instead of a high-quality analogue sine wave, an adapted pulse is applied to obtain the signature result, which is more appropriate to implement in a multi-site testing environment. In this chapter, we propose a machine-learning-based test for ADC, estimating both the dynamic and static specifications based on the *ORP*.

This chapter is organized as follows. In section 5.3, the basic concept of machine-learning-based testing is explained. The proposed test methods predicting dynamic and static specifications of ADCs are introduced in section 5.4 in detail. As the prediction results of the SNR are not sufficiently accurate, an improved method is proposed in section 5.5. The simulation results and analysis of the proposed test methods of the 12-bit pipelined ADC are presented in section 5.6. In this section the prediction of both fault-free and faulty devices are investigated. The measurement results of the 12-bit pipelined ADCs are shown in section 5.7. Finally the conclusions are given in section 5.8.

5.3 Basic concept of testing via machine-learning

The basic concept of machine-learning-based testing is shown in Figure 5.1. As depicted in the figure, one can obtain the results of the desired parameter by signature measurements. The approach to link them is using a mapping function based on their strong correlation. In contrast with conventional testing, machine-learning-based testing obtains the results of the specifications of the DUTs in an indirect way. Instead of the specifications, the signature results are measured with unconventional test stimuli or post-processing methods. The key issue in machine-learning-based testing is that the signature results must have a strong *correlation* with the specifications. In such a case, a mapping function can be built by training with a set of known good devices. Once the mapping function is constructed, the specifications can be estimated from the signature results.

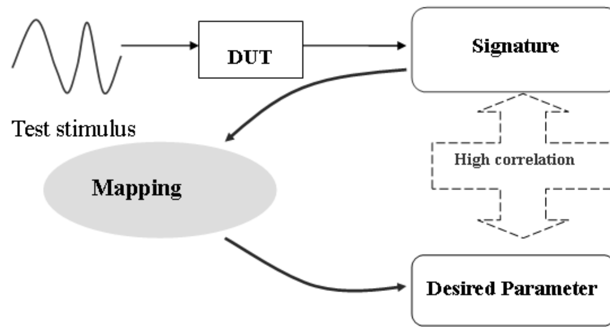

Figure 5.1: Basic concept of machine–learning-based testing

Usually, the MARS algorithm is selected to build the mapping function, being popularized in 1991 by Friedman [Fri91]. One can consider it as an extension model from the linear regression model with more flexibility. The main purpose of the MARS analysis is to predict a dependent variable from a set of independent predictor variables. It builds the model described as in [Fri91]:

$$\hat{f}(x) = c_0 + \sum_{i=1}^{k} c_i B_i(x) \tag{5.1}$$

where x is the predictor variable, $B_i(x)$ denotes the so-called basic function, c_i represents a constant coefficient and $\hat{f}(x)$ is the dependent variable. The hat on the $\hat{f}(x)$ indicates that $\hat{f}(x)$ is an estimated value. Each basic function takes one of the next three forms: a constant 1, a single hinge function and a product of two or more hinge functions. A hinge functions can be defined as follows:

$$y = \max(0, x - c) \quad or \quad y = \max(0, c - x) \tag{5.2}$$

where c is a constant. When building the model, the value of c is automatically selected by the MARS algorithm. The MARS model is a weighted sum of the basic function. The MARS algorithm selects a set of basic functions to maximize an overall least-squares goodness-of-fit criterion [Kim07]. The MARS algorithm then searches over the space of all inputs and predictor values as well as interactions between variables. During this search, an increasingly larger number of basic functions are added to the model. As a result of these operations, MARS automatically determines the most important independent variables as

well as the most significant interactions among them. The implementation of the MARS algorithm can be downloaded from the Internet [Var].

5.4 Prediction of dynamic and static specifications with a pulse-wave stimulus

An overview of our machine-learning-based test method is shown in Figure 5.2. First, a set of ADCs is selected as the training set. The test results of the training set are used for building the mapping function. For an accurate prediction of the specifications, it is recommended that the training set covers all corner cases (typical, fast and slow).

Second, each device in the training set has to be tested twice. The first time, it is tested via the pulse-wave input signature-based testing approach. The second time, it is tested with the conventional sine-wave input testing method. Both the signature and specification results are required as the training data.

Third, after collecting both the signature as well as the specification results, a mapping function can be built by using the MARS algorithm. This function can map the signature results to the specification space under the condition of strong correlation.

During mass-volume testing, only the signature-based testing is applied to the DUTs. Once the signature results are obtained, the estimated specifications can be calculated by the previously constructed mapping function. The details of the whole process will be discussed later.

In our approach, a pulse wave with noise and non-linear edges is applied as a realistic test stimulus for all the DUTs. Obviously, such a low-quality pulse wave is easier and less expensive to generate than a high-quality analogue sine wave as used for conventional testing. Nowadays more and more ADCs are integrated into a platform-based design, which often contains digital parts like memories and multiple processor-cores. As discussed in chapter 3, while using a pulse wave as the test input signal, the rising and falling edges should be set properly; at least larger than the reciprocal of the sampling frequency of the ADC. The flow is now as follows:

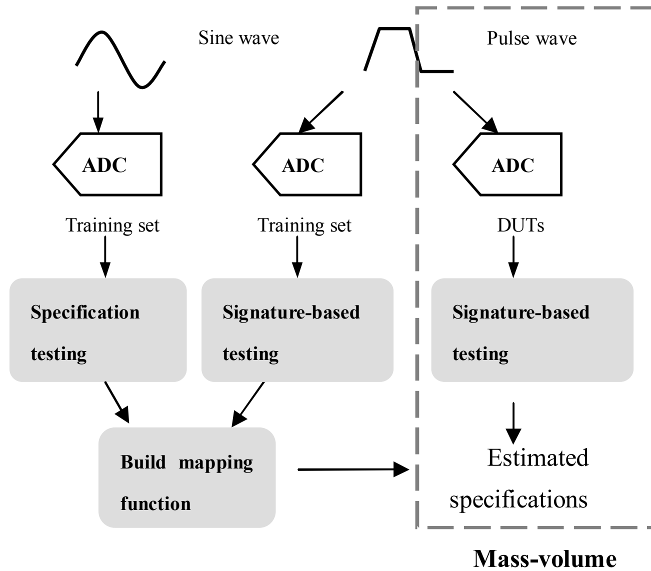

Figure 5.2: Overview of the proposed test method

1. Conventional specification-based testing of the training set

The desired conventional dynamic specifications, SFDR, THD, SINAD and SNR are measured by the conventional test method using an analogue pure sine wave and FFT post calculation. The conventional static specifications, DNL and INL are measured by using a high-quality sine wave or a ramp signal.

2. Signature-based testing for the training set

The flow of signature testing is shown in Figure 5.3. In the previous chapter, we proposed signature testing to distinguish the faulty devices from the fault-free devices by the signature *ORP* in amplitude. This is an analysis in the time domain, which is simpler than the FFT analysis in conventional testing. The basic idea is using the *ORP* to define the similarity between the outputs of the golden devices (fault-free devices defined by the specification testing) and the DUTs. Based on the degree of similarity, the faulty devices can be distinguished. In this work, the signature testing included in the machine-learning-based testing is based on the signature *ORP* but with some differences. This is because the *ORP* is now used as a variable to predict the actual specifications. In the original work, a certain amount of golden devices are used as reference devices, which have to be fault-free. In this

approach, the training devices are used as the reference devices. However, they do not have to be all fault-free.

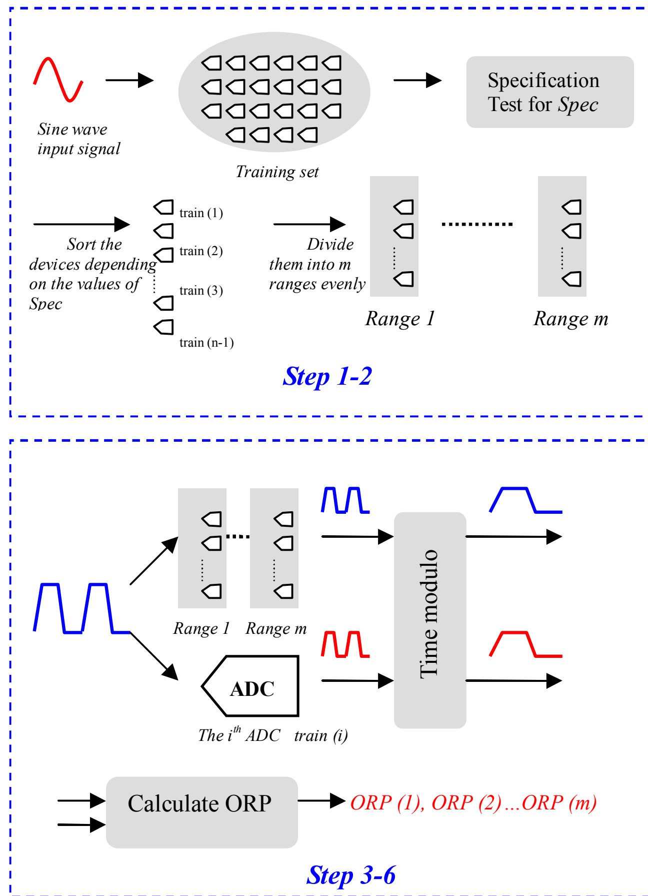

Figure 5.3: The flow of our signature-based test

The specific steps are explained as follows:

Step 1: Assume the specification parameter *Spec* (for example, the THD) is the required parameter to be predicted by the signature results later. All the values of *Spec* of the training set can then be sorted in ascending or descending order. After that, an array of *Spec* can be obtained:

$$Spec(1), Spec(2)\ldots Spec(i)\ldots Spec(n).$$

The parameter n is total number of the ADCs in the training set. The corresponding

training device of each *Spec (i)* can be represented as *train (i)*.

Step 2: Divide all the elements in the array *Spec* evenly into a number of ranges. If there are m ranges as shown in Figure 5.3, then these ranges will be: $\left[Spec(1), Spec(1+\lfloor n/m \rfloor)\right]$, $\left[Spec(1+1*\lfloor n/m \rfloor), Spec(1+2*\lfloor n/m \rfloor\right], \ldots$

Here the $\lfloor n/m \rfloor$ indicates the largest integer not greater than n/m.

Step 3: As shown in Figure 5.3, pulse waves with the same period, amplitude, rising and falling edges are applied to all the ADCs in the training set. By applying the time-modulo plot [Iro96] to the output, the number of periods of pulse waves can be transferred to only one period waveform without losing any test information. This technique shows the output waveform in a more clear and simple way for later analysis [She09]. For each device, an array of the output amplitude can then be obtained as: *Am (1), Am (2), Am (3)... Am (N)*. Each element *Am (i)* represents the amplitude of one sample point on the output curve. N is the number of sample points of the output.

Step 4: For each range defined in step 2, the maximum amplitude $Am_{max}(i)$ and minimum amplitudes $Am_{min}(i)$ of each sample point can be determined. They are obtained by comparing the output amplitude of the corresponding devices of each range. The acceptable amplitude range of the ith sample point of one certain range can then be defined as $[Am_{min}(i), Am_{max}(i)]$.

Step 5: Verify if each amplitude element *Am (i)* of one ADC in the training set is within the range $[Am_{min}(i), Am_{max}(i)]$. If it is within the range, the deviation from the range $\triangle Am(i)$ is defined as zero. Otherwise, it is defined as:

$$\Delta Am(i) = Am(i) - Am_{\max}(i), \text{ if } Am(i) \text{ is larger than } Am_{max}(i). \tag{5.3}$$

On the other hand,

$$\Delta Am(i) = Am_{\min}(i) - Am(i), \text{ if } Am(i) \text{ is smaller than } Am_{min}(i). \tag{5.4}$$

Step 6: After completing the collecting, the deviation of all the sample points for one certain range, the *ORP* of one ADC, can be calculated as [She09]:

$$ORP = \frac{\sum_{i=0}^{N} \Delta Am(i)}{\sum_{i=0}^{N} Am_{\max}(i) - \sum_{i=0}^{N} Am_{\min}(i)} \tag{5.5}$$

If there are m ranges in total, then m different *ORP*s can be obtained being: *ORP (1), ORP (2)…ORP (m).*

3. Building the Mapping Function

After the signature-based testing of the training set, the MARS algorithm is used to build up a mapping function. As shown in Figure 5.2, the inputs of the algorithm are the specification measurements and the corresponding signature *ORP* measurements of the training set. Later on, a mapping function that can map the *ORP* to the specification measurements can be extracted. The ORP has to be calculated for each specification (SNR, THD, SINAD, SFDR, INL or DNL) respectively. Therefore, for a different specification, the mapping function also needs to be extracted subsequently.

4. Signature-Based Testing for the DUTs

In the case of calculating the *ORP* of the DUTs, the same methodology as the training set is exploited. The test input signal has the same settings as the signature testing of the training set. In contrast to the signature testing of the training devices, only the steps 3, 5 and 6 are carried out on the DUTs. The acceptable ranges of the amplitudes for calculating the *ORP* are still the ones obtained from the training set.

5. Estimate the specifications of the DUTs

At the end, one can just substitute the variables of the mapping function with the *ORP* values of the DUTs. The results of the mapping function will be the estimated values of the corresponding specifications. For example, as shown in Figure 5.4, the ORP_{INL} is the signature result obtained for INL estimation. After substituting this result into the corresponding mapping function, the estimated INL results can be calculated.

Figure 5.4: Example of the estimation of the INL from ORP_{INL}

5.5 Improvement of SNR in machine-learning-based testing

In the proposed machine-learning-based test method, the simulation results shown later, indicate that the prediction of the SNR turns out not to be sufficiently accurate. For this case, we propose a method for improving the accuracy of the SNR prediction in this section.

Besides the noise caused by the ADC circuitry, the output of the ADC also contains noise of the input signal. The conventional specification testing requires that the input test stimulus is very pure. Therefore, the output would contain more pure test data of the DUT itself. However, in the previous machine-learning-based method, a noisy pulse wave is applied as a realistic low-quality input test signal. As the noise of the input stimulus is comparable with the noise of the ADC circuitry, it becomes a considerable part of the SNR value. Consequently, it could mask the real noise caused by the DUT. This is the reason why an input pulse wave with 3 LSB noise cannot predict SNR accurately of a 12-bit pipelined ADC as shown in later simulation results. In order to decrease the influence of the noise from the input signal, an improved method is proposed. In [Cau00], a two-ADC method is proposed to improve the SNR results of the conventional specification test. However, an analogue sine wave and the FFT analysis are required as the test stimulus and post-processing method respectively. It is very difficult to apply completely the same input signal (including noise) to two ADCs in a real production environment. Therefore, to start our investigation, the same input stimulus is applied to two ADCs in the simulation.

Based on the work in [Cau00], this approach is now applied to signature testing, which exploits a pulse-wave input signal and time-domain post-processing.

In our original machine-learning-based test method, the output data is reorganized into one single period for calculating the signature *ORP*. Now, the output is reorganized into a double-period output waveform as discussed in their method [Cau00].

The one-period waveform is now subtracted from the other. In this way, the systematic error of the ADC is removed from the output (like nonlinearities and quantization errors) as it is a repeatable error. If one assumes there are two ADCs tested with the same input stimulus, named 'ADC1' and 'ADC2', their subtracted outputs of the two periods can be expressed respectively as:

$$\sigma_1^2 = \sigma_{ADC1}^2 + \sigma_{signal}^2 \tag{5.6}$$

$$\sigma_2^2 = \sigma_{ADC2}^2 + \sigma_{signal}^2 \tag{5.7}$$

where σ_{ADC1}^2 and σ_{ADC2}^2 represent the variance of the noise from the outputs of ADC1 and ADC2 respectively and σ_{signal}^2 represents the variance of the noise induced by the input stimulus.

Subsequently, the differential output between σ_1^2 and σ_2^2 is computed, which can be represented as:

$$\sigma_3^2 = \sigma_{ADC1}^2 + \sigma_{ADC2}^2 \tag{5.8}$$

From equations 5.6, 5.7 and 5.8, σ_{ADC1}^2 and σ_{ADC2}^2 can be computed. They can be exploited as an additional signature to predict the SNR in the machine-learning-based method. As result, not only *ORP* but also σ_{ADC1}^2 and σ_{ADC2}^2 are used to build up the mapping function. In this way, it is possible that the mapping function can map the signatures to the SNR more accurately. It will result that the SNR will be estimated more accurately.

5.6 Simulation results and analysis of the Labview model of a 12-bit pipelined ADC

A 12-bit pipelined ADC has been used to validate the proposed machine-learning-based test method. As described in Chapter 3, in the Labview model of the 12-bit pipelined ADC, there are several key parameters that can affect the performance of the ADC:

- The reference voltages of the comparators in the flash ADC of each sub-stage
- The values of the capacitors in the MDAC of each sub-stage
- The gain of the residue amplifier in the MDAC of each sub-stage

These parameters will change depending on the process variations in the fabrication. For this reason, independent Gaussian noise sources are added to all these key parameters

respectively. As a result, the values of these parameters are generated randomly to emulate the devices with the process variations. The range of values is suggested by the designer of the 12-bit pipelined ADC.

5.6.1 Simulation setup

In the simulation of the proposed method, 2000 training devices are used to build mapping functions and 1500 test devices are used to evaluate the method. All devices in the simulation are generated randomly by adding Gaussian noise to the key parameters of the ADC model. The specification is tested using a perfect sine wave of frequency f_{in}=38 MHz, a sampling frequency f_s=80 MHz and the number of samples is N=4096.

The input stimulus can be represented as:

$$x(t) = v_{os} + \eta\left[t + 0.04 * (t^2 + t)\right] + n(t) \tag{5.9}$$

where $x(t)$ represents the amplitude of the slope of the pulse wave, v_{os} denotes the offset voltage, η represents the slope and $n(t)$ is the noise. The part $0.04*(t^2-t)$ corresponds to the 7-bit nonlinear property of the slope of the input pulse wave. Gaussian white noise has been added to the entire pulse wave. The Gaussian white noise is from the module in Labview, which provides an ideal white noise with infinite bandwidth. All the simulations have been performed with an adapted pulse-wave of input frequency f_{in}=38 MHz, rising or falling time $t_r = t_f$= 6 ns, a sampling frequency of f_s=80 MHz, and the number of samples is N=4096.

The MARS algorithm has been applied by using existing software [Jek10]. It has two functions:

1. Build the mapping function from the specifications and the signature results from the training data.
2. Predict the specifications of the DUTs by the signature results and the mapping function constructed in 1.

In signature testing, the number of ranges m determines how many variables there are in the mapping function. In order to see its impact on the estimated specifications, different values of m have been applied in the simulations to be discussed next.

5.6.2 Simulation results and analysis of the prediction of *dynamic* parameters of fault-free 12-bit pipelined ADCs

In the simulations on dynamic parameters, four dynamic parameters SINAD, THD, SFDR and SNR have been predicted. We first only investigate the prediction of dynamic parameters of fault-free devices. As a result, both 2000 training devices and 1500 test devices are fault-free devices. In the next section, the prediction of faulty devices will also be discussed. A pulse wave of 7-bit nonlinear edges and noise with a standard deviation $\sigma = 0.8$ LSB has been applied. The simulation results for the four dynamic parameters are shown in Figures 5.5-5.8 respectively. As shown in the figures, all predicted values are calculated by a mapping function with 30 variables (30 *ORP*). The x-axis denotes the simulated dynamic parameters by using a pure sine wave stimulus and FFT calculations while the y-axis denotes either the actual or estimated values. The straight lines plot the actual values of the specifications and the stars plot the corresponding estimated values. From the figures, one can observe that the predicted values seem quite close to the actual values.

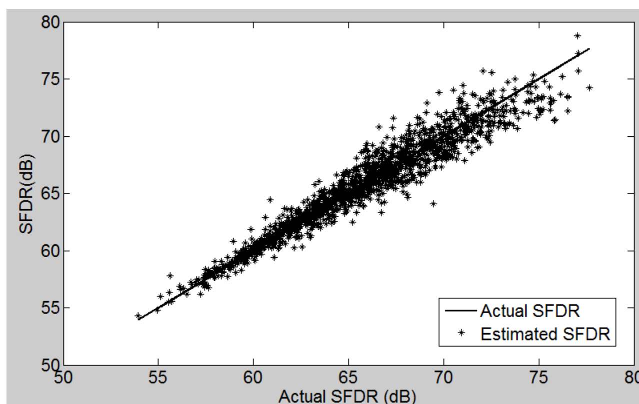

Figure 5.5: The SFDR simulation results with a mapping function of 30 variables (1500 test devices)

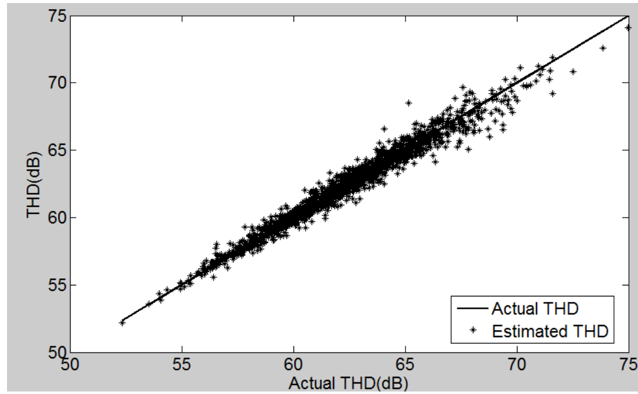

Figure 5.6: The THD simulation results with a mapping function of 30 variables

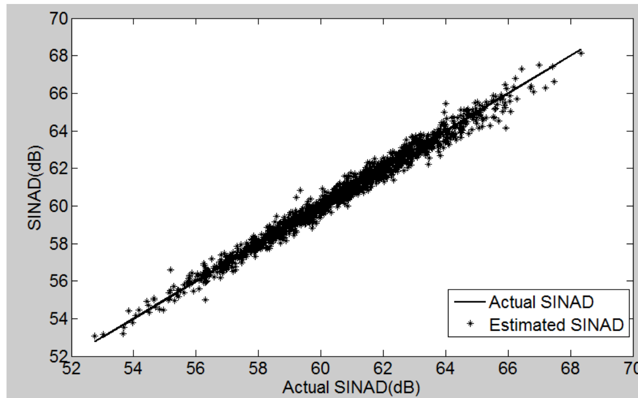

Figure 5.7: The SINAD simulation results with a mapping function of 30 variables

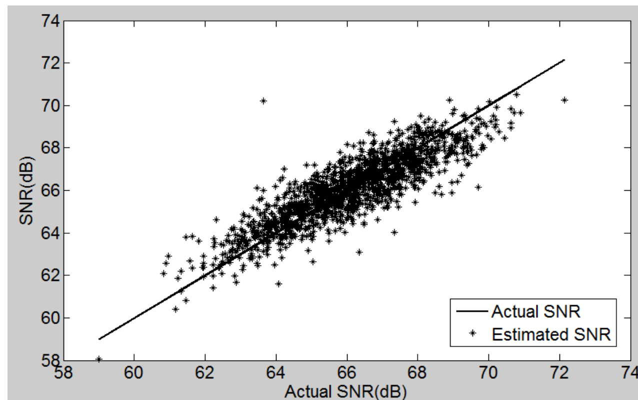

Figure 5.8: The SNR simulation results with a mapping function of 30 variables

In order to evaluate the results in a more accurate way, the error is defined as the deviation between the actual values and the estimated values. In the production test of mixed-signal circuits, the concept of correlation defines the ability of obtaining the same results when testing the same device with different hardware or software. However, in reality it is very hard to obtain completely identical results as the test environment can never be perfect. In general, it is sufficiently accurate to ensure that the deviation of the results is less than one-tenth of the full range between the minimum test limit and maximum test limit [Bur00]. According to this requirement, if the error is smaller than one-tenth of the full range of the specification, the estimated result is defined as being acceptable. On the other hand, we define the case in which the error is larger than one-tenth of the full range, as an outlier.

In Table 5.1, the mean error and the number of outlier cases are presented. They are all obtained by a pulse-wave stimulus with 7-bit nonlinear edges and a noise of σ = 0.8 LSB. From Table 5.1, one can observe that if there are 30 variables in the mapping function, the estimated results are the most accurate. In signature testing, one tries to divide the training devices into a different number of ranges *m*. By increasing the number of ranges, more *ORP*s are calculated for each device. Therefore, the number of variables of the mapping function increases as well. In this way, the model built by MARS can fit the relationship between the specifications and the signature in a better way. In case the number of variables increases over 30, it does not improve the results too much. Moreover, it increases the time of building the mapping function. For these reasons, 30 variables were chosen to build the mapping function in the end.

Table 5.1: The errors and outliers in the estimated dynamic results with different number of variables in the mapping function (2000 training devices)

Input pulse wave of 7-bit nonlinear edges and a noise with σ = 0.8 LSB				
		2 variables	**15 variables**	**30 variables**
SFDR	Mean error (dB)	1.70	0.78	0.68
	Number of outliers	131	6	11
THD	Mean error (dB)	1.12	0.43	0.38
	Number of outliers	192	4	1
SINAD	Mean error (dB)	0.68	0.31	0.23
	Number of outliers	73	9	2
SNR	Mean error (dB)	1.22	0.78	0.66
	Number of outliers	629	270	120

As shown in Table 5.1, the mean errors obtained by 30 variables are 0.68, 0.38, 0.23 and 0.66 dB for the SFDR, THD, SINAD and SNR respectively. The ratios between the mean errors to the full range of the specifications are 2.4%, 1.6%, 1.4% and 4.6%. In another words, the results are completely within the requirement that the error should be smaller than one-tenth of the full range of the specifications. However, there are still outliers, the error of which is larger than one-tenth of the full range. All these outliers can cause yield loss in production testing. For the SNR, the number of outliers is considerable being 120 out of 1500 DUTs (8% of the DUTs), compared with typical yield loss. However, the number of outliers of the SFDR, THD and SINAD is relatively very small to 1500 DUTs as shown in Table 5.1. The ratio between their outliers to the total number of the DUTs is not larger than 0.8%, which is small compared with nominal values of yield loss [Cip01].

In Table 5.2, the estimated results with different standard deviation σ of the noise of the input signal are presented. From the Table, one can observe that the mean error becomes larger as the standard deviation of the noise increases. However, they are all within 10% of

the full range of the specifications. The number of the outliers from the SFDR, THD and SINAD are still relatively small when increasing the noise. For the SNR, the ratio between the outliers to the total number of DUTs is too large to be acceptable, although the mean error can satisfy the requirement. Among all the dynamic parameters, the SNR always has the worst prediction. Noise is a random error source. In our signature testing, a set of devices is used as reference to calculate the *ORP*, which has the random noise error as well as the noise of the DUTs. As a result, the *ORP* can reflect the noise error to a certain degree but not sufficiently accurate. The SINAD, as well as SNR which includes the noise information, can have an accurate estimated result. This is because the values of the harmonics are relatively dominant with respect to the noise in the calculation of the SINAD. In our case, the mean value of the harmonics is 5 dB higher than the noise.

In order to evaluate the time required for the data-processing, both the FFT analysis and the proposed signature test algorithm have been carried out in Matlab programs on the same computer. Their computation time is 0.076 s and 0.01 s respectively. Obviously, the data-processing involved in signature testing consumes much less time.

Table 5.2: The errors and outliers in the estimated dynamic results with different input stimulus noise

Input pulse wave of 7-bit nonlinear edges, 30 variables in the mapping function				
	Input noise	**σ= 0.2 LSB**	**σ= 1.6 LSB**	**σ= 3 LSB**
SFDR	Mean error (dB)	0.67	0.69	1
	Number of outliers	10	4	45
THD	Mean error (dB)	0.38	0.49	0.77
	Number of outliers	5	4	18
SINAD	Mean error (dB)	0.24	0.35	0.66
	Number of outliers	3	0	25
SNR	Mean error (dB)	0.72	0.88	1.07
	Number of outliers	315	352	522

5.6.3 The Simulation results and analysis of the *dynamic* parameters of a 12-bit pipelined ADCs *with faults*

In the previous simulations with regard to dynamic parameters, only the fault-free ADCs are used to validate if the machine-learning-based test method can obtain accurate specification results. However, whether the method can distinguish the faulty devices from the fault-free ones also needs to be validated. In our case, the faulty devices are randomly generated by changing the settings of the white Gaussian noise, which has been already injected into the Labview model of the ADC. With different standard deviations of the white Gaussian noise, 3 different test sets are obtained. Each test set contains 1500 devices but with a different number of faulty devices.

The predicted results of the 3 test sets are listed in Table 5.3. It lists the mean values of the dynamic parameters, test escape and yield loss, which have been already defined in section 4.8. In Table 5.3, while comparing the results of the 3 test sets, one can observe that as the

mean values of the dynamic parameters become increasingly deviating from the fault-free range it means there are more faulty devices in the test set. Comparing all dynamic parameters, the THD results in the smallest yield loss and test escape. In Table 5.2, the THD also results in the smallest number of outliers in the case there are only fault-free devices. As a result, the proposed method can predict THD results better than the other dynamic parameters. In Table 5.3, apparently the proposed testing has some yield loss and test escape compared with the conventional testing. The SFDR has the largest test escape 7.2%. For the THD, SNR and SINAD, the test escape or the yield loss are not larger than 2.4%. The predicted results of the proposed method can match the results of conventional testing very well.

Table 5.3: The estimated dynamic parameters of ADCs with faults

		Test set 1	**Test set 2**	**Test set 3**
SFDR fault-free range [52.54, 80.21]dB	Mean (dB)	52.49	47.31	38.61
	Std. deviation (dB)	5.26	6.66	5.74
	Yield loss	1.9%	1.3%	0.2%
	Test escape	7.2%	6.5%	2.3%
THD fault-free range [74.78, 52.06]dB	Mean (dB)	53.84	45.86	37.48
	Std. deviation (dB)	5.3	6.14	5.53
	Yield loss	1.1%	0.6%	0
	Test escape	0.80%	1.5%	0.67%
SNR fault-free range [52.52, 71.29]dB	Mean (dB)	58.42	50.13	40.94
	Std. deviation (dB)	5.46	6.62	5.95
	Yield loss	0.47%	0.73%	0.2%
	Test escape	0.8%	1%	2.4%

SINAD fault-free range [51.78, 68.65]dB	Mean (dB)	52.49	44.46	35.85
	Std. deviation (dB)	5.26	6.25	5.64
	Yield loss	1.1%	0.47%	0.27%
	Test escape	1%	1.2%	1.5%

5.6.4 The simulation results and analysis with an improved method for SNR prediction

As discussed before, the results of SNR are not sufficiently accurate. Therefore, an improved method of testing SNR has been proposed. In this section, the simulation is carried out to validate this proposed method. The simulation setup is the same as presented in section 5.6.1. In the original method, 30 variables are selected to build up the mapping function for predicting the SNR. In the improved method, the 30 variables are kept the same, but one more variable σ^2_{ADC} is added to the mapping function as discussed in section 5.5. A white Gaussian noise with a standard deviation $\sigma = 3$ LSB is added to all input test stimuli. The simulation result is shown in Figure 5.9. The x-axis denotes the reference values of the SNR simulated with a perfect sine wave while the y-axis denotes the SNR values from different data series. The grey circles plot the estimated SNR in our previous work while the black dots plot the estimated SNR by the improved method. One can observe that the black dots are more close to the straight line, which is the reference SNR value obtained by a perfect sine wave.

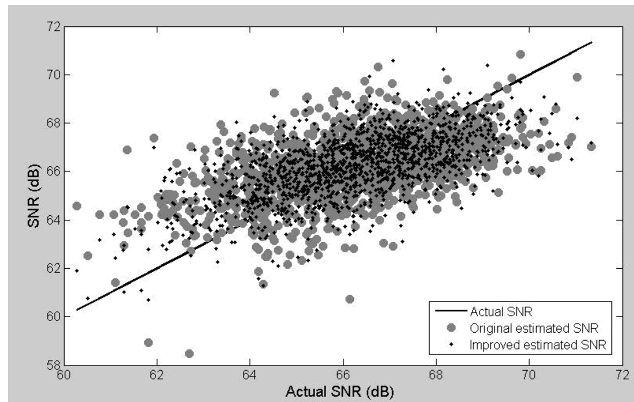

Figure 5.9: The SNR simulation results with original and improved machine-learning -based test methods

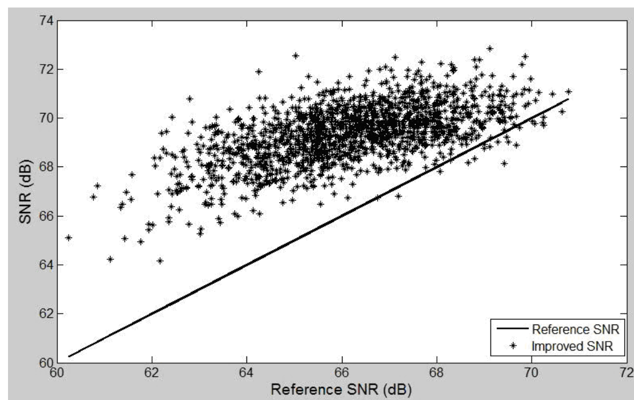

Figure 5.10: SNR estimation results with original double-ADC method in [Cau00] **using noisy sine stimulus and FFT calculation**

The proposed improved method is based on the method in reference [Cau00]. The simulation of the original method in [Cau00] has also been carried out. It is applied to the 1500 test devices, which uses the perfect sine wave as the test stimulus without using the machine-learning-based test method. The same Gaussian white noise as in the pulse-wave approach has also been added to the input sine wave. The simulation results are shown in Figure 5.10. There are two data series in Figure 5.10. One consists of the reference SNR values obtained by the perfect sine wave and the other one is the SNR values obtained by a noisy sine wave. If one compares the result in Figure 5.10 with the one in Figure 5.9, our results in Figure 5.9 have obviously a much better accuracy.

The mean error and outliers in both Figures 5.9 and 5.10 are listed in Table 5.4. One can conclude that the improved machine-learning-based method obtains the most accurate results.

- Compared with the previous machine-learning -based test method, adding one more variable to the mapping function (the improved method) decreases the mean error by 0.12 dB and the number of outliers by 54. Obtaining the extra variable only requires an additional FFT computation for post-processing.
- Compared with the original double-ADC method, the mean error of the improved machine-learning method is 2.24 dB better and the number of outliers is 460 less. With the same level of input noise, the latter method can obtain much more accurate results. The double-ADC method requires an analogue sine-wave input signal while the improved machine-learning-based method only requires the adapted pulse wave.

Table 5.4: The estimated dynamic parameters of ADCs with faults

SNR results	Mean error (dB)	Number of outliers
Original machine-learning -based method	1.07	522
Improved machine-learning -based method	0.95	468
Double ADC method [Cau00]	3.19	928

5.6.5 Simulation results and analysis of the *static* parameters of 12-bit pipelined ADCs

The static parameters INL and DNL, which are the most difficult to test of all static parameters, have been predicted in our simulations. The same pulse wave as the one for

testing the dynamic parameters is applied as test stimulus. However, as a starting point, it is without any noise and non-linearity. There are 30 variables used to predict the static parameters. The simulation results are shown in Figures 5.11 and 5.12. The x-axis denotes the reference values of the static parameters and the y-axis denotes the estimated values. From the figures, one can conclude that neither the estimated INL nor the DNL are very close to the actual results. The results in the figures are summarized in Table 5.5. One can observe that the ratios between the outliers with respect to the total number of the DUTs are 22% and 81% for the INL and DNL respectively. This is obviously not acceptable. As a consequence, the proposed method is not suitable for testing the static INL and DNL parameters.

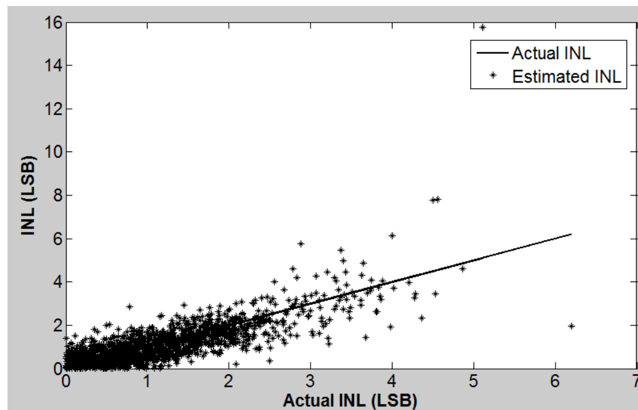

Figure 5.11: The INL simulation results with a mapping function of 30 variables using machine–learning–based testing

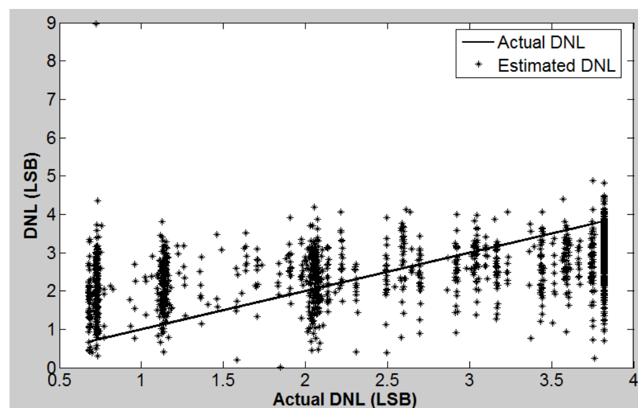

Figure 5.12: The DNL simulation results with a mapping function of 30 variables using machine–learning–based testing

Table 5.5: The errors and outliers in the estimated static results by the machine-learning-based test method

	Mean error (LSB)	Max error (LSB)	Number of outliers
INL	0.42	10.65	325
DNL	0.89	8.25	1210

5.7 Measurement setup and results of a 12-bit pipelined ADC

In the previous simulations, 2000 training devices are used to build the mapping function and 1500 test devices to validate the method. However, in real measurements, there are only 109 devices available, which have all been manufactured on the same wafer. We divide them into two sets: a training set and a test set. The ratio between the number of training devices and the test devices is the same as the one in the simulation. In this case, 63 devices are randomly selected as the training devices and the remaining 46 test devices are used to validate the test methods. All DUTs have been tested by two main measurements approaches:

1) Conventional testing

The dynamic specifications of the ADCs are measured using a sine wave with an input frequency of 1.8 MHz, which is generated by a 16-bit arbitrary waveform generator (AWG). The number of samples is 16384 and the sampling frequency is 25 MHz. The THD, SNR, SINAD and SFDR are calculated using the FFT analysis.

2) Signature testing

In the signature testing approach, five different pulse waves have been applied as the test stimulus respectively, in order to investigate the robustness of the method. Their settings are listed in Table 5.6.

Table 5.6: Settings of different pulse input stimuli for signature testing

	Input frequency (MHz)	Duty cycle (%)	Rise & fall times (ns)	Linearity of slope (bits)	Number of samples
Pulse 1	1.8	50	100	16	16384
Pulse 2	1.8	50	50	16	16384
Pulse 3	1.8	50	25	16	16384
Pulse 4	1.8	50	100	12	16384
Pulse 5	1.8	50	100	7	16384

After completing both conventional testing and signature testing, the data from the 64 training devices are used to build the mapping function by using the MARS algorithm. The signature results from the 46 testing devices are used to estimate the dynamic specifications. It is the same as being used in the simulations that different variables are tried to build up the mapping function. Finally, we select 16 variables in the mapping function. Next the estimated results are compared with the measured results.

In order to better evaluate the estimated results, the specification testing for each device is repeated ten times [Goy07]. The standard deviation and 3-sigma are calculated by One-Way Analysis of Variance [Ano]. They are shown in Table 5.7. The 3-sigma value can be interpreted as the maximum error of conventional specification testing [Goy07]. Here we define that the estimated results of which the error is larger than the maximum error, are considered to be outliers.

Table 5.7: Standard deviation and 3-sigma value of the conventional specification-based test method

	Std. deviation	3-sigma
THD (dB)	0.43	1.29
SNR (dB)	0.06	0.18
SINAD (dB)	0.07	0.21
SFDR (dB)	0.77	2.31
INL	0.24	0.72
DNL	0.09	0.27

5.7.1 Measurement results and analysis of the dynamic parameters of a 12-bit pipelined ADC

In Figures 5.13-5.16, the estimated results obtained by *pulse 5* are shown, which has only a 7-bit linearity. In these figures, the x-axis denotes the reference values of the dynamic specifications tested by the specification-based testing approach. The y-axis denotes the values of the dynamic parameters from different data series. The straight line denotes the upper and lower limits of the tolerance of the estimated results, which are the reference values minus or plus the 3-sigma value. The black dots are the reference values of the dynamic parameters while the black stars are the estimated results of the dynamic parameters. Compared to the simulation results in Figures 5.5-5.8, the results in Figures 5.13-5.16 show very poor correlation between the estimated results and the conventional measurement results. It means the proposed method in the measurement can not predict the dynamic parameters very well. In order to further analyze the results, the mean error and outliers are also calculated and shown in Table 5.8. The error is defined as the deviation between the estimated values and the reference values. The estimated result is defined as the outlier if it is out of the +/- 3sigma of the mean value. One can notice that these 5 different pulse waves result in similar mean errors and number of outliers. For THD, SINAD and SFDR, all pulse waves obtain a significant number of outliers. As a result, the accuracy of the estimated results is not acceptable. The number of outliers in the case of SNR is smaller. However, as

the correlation between the estimated results and reference results is poor, the small number of outliers still cannot guarantee that the proposed method can correctly estimate the SNR of the ADC.

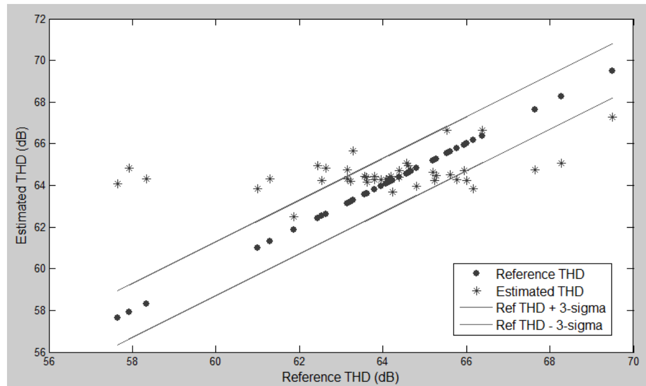

Figure 5.13: The estimated results of the THD with input *pulse 5*

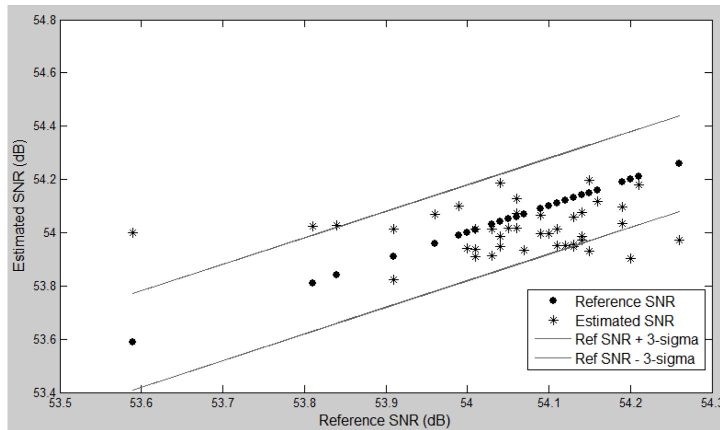

Figure 5.14: The estimated results of the SNR with input *pulse 5*

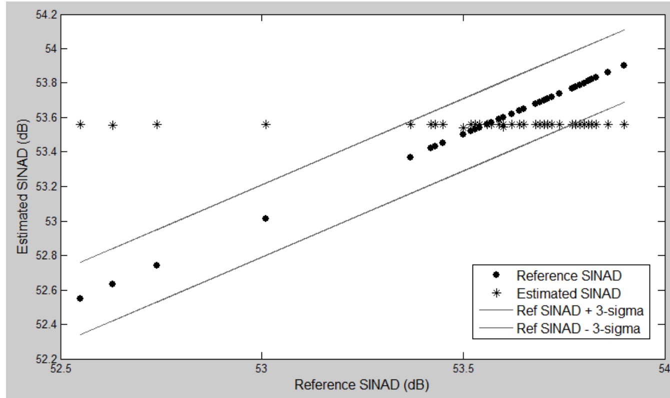

Figure 5.15: The estimated results of the SINAD with input *pulse 5*

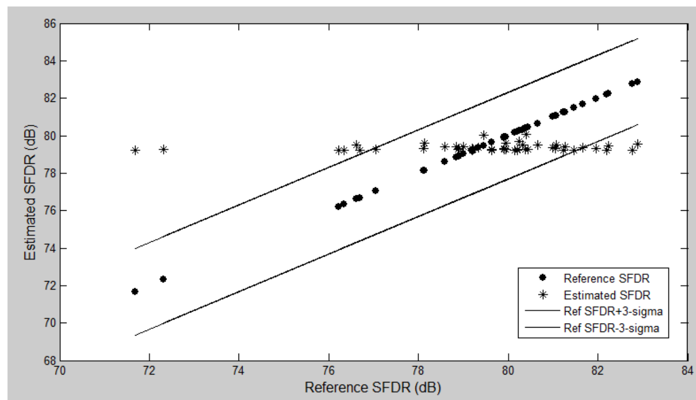

Figure 5.16: The estimated results of the SFDR with input *pulse 5*

Table 5.8: The mean error and outliers in the estimated dynamic results with different standard deviation of the noise of the input signal in measurements

		THD	SNR	SINAD	SFDR
Pulse 1	Mean error (dB)	1.60	0.12	0.2	1.59
	Number of outliers	18	5	12	10
Pulse 2	Mean error (dB)	1.61	0.12	0.21	1.59
	Number of outliers	19	7	11	11
Pulse 3	Mean error (dB)	1.62	0.11	0.2	1.58
	Number of outliers	18	6	11	12
Pulse 4	Mean error (dB)	1.62	0.11	0.21	1.58
	Number of outliers	16	7	12	12
Pulse 5	Mean error (dB)	1.53	0.12	0.2	1.59
	Number of outliers	16	6	12	10

Besides using the number of outliers to evaluate the results, the so-called *correlation coefficient* is also interesting to use in this case. It can indicate the correlation between the reference results and the estimated results. By using the function *corrcoef* in Matlab, one can obtain the correlation coefficient of the results in Figures 5.5~5.8 as shown in Table 5.9. The number of outliers in Table 5.9 is taken from Table 5.1. From the simulation results of Figures 5.5~5.8, it was concluded that the number of outliers is too large to be acceptable for SNR case. For the THD, SFDR and SINAD, the number of outliers is acceptable. As a result, one could define that if the correlation coefficient is larger than 0.96, the estimated results are acceptable; if the correlation number is smaller than 0.87, the estimated results are not acceptable.

Table 5.9 Correlation coefficient of simulated dynamic parameter results from Figure 5.5~5.8

Dynamic parameter	Number of outliers	Correlation coefficient
THD	1	0.98
SNR	120	0.87
SFDR	11	0.96
SINAD	2	0.99

The correlation coefficients of the results in Figures 5.13~5.16 can also be calculated and are shown in Table 5.10. From the number of outliers, one can conclude that the estimated results of all the dynamic parameters are not acceptable. In Table 5.10, one can see that the correlation coefficients are all smaller than 0.87. Hence, while using the concept of correlation coefficients one can come to the same conclusion being that the measurements cannot be predicted by the proposed method.

Table 5.10 Correlation coefficient of measured dynamic parameter results from Figures 5.13~5.16

Dynamic parameter	Outliers	Correlation coefficient
THD	16	0.41
SNR	6	0.14
SFDR	10	0.3
SINAD	12	0.38

From the analysis of the measurement results, one can conclude that the proposed method cannot predict the dynamic parameters correctly. This conclusion is completely opposite to the one from simulation. Compared to the simulation, the most obvious difference is the number of training devices. In the simulation, there are 2000 training devices while there are

only 64 training devices in the case of measurements. Insufficient training data can not build up an accurate mapping function between the dynamic specifications and the signature results. It is possible that the 64 training devices are not sufficient to build up an accurate mapping function. The most direct way to verify this is to use also 2000 training devices in the measurement. However, unfortunately we do not have so many devices. In this case, we can only verify it based on simulations. In the simulations, the number of training devices and test devices are changed to the same number as in the case of the measurements. The number of variables is also taken the same as in the measurements. As an example we only select one typical dynamic parameter THD for the investigation, as all dynamic parameters show a similar behavior in the proposed method. Figure 5.17 shows the simulation results of the THD obtained from 63 training devices and 46 test devices. Compared to the simulation results of the THD in Figure 5.6, the correlation between the reference THD and estimated THD is obvious much worse. In order to further investigate this issue, more simulations have been carried out. In these simulations, the number of training devices is increased from 250 to 2000. The ratio between the training devices and the test devices is always the same as in the measurement. The number of variables is kept to 16 in the mapping function. In order to evaluate the correlation between the estimated and reference results, the well-known *correlation coefficient* is exploited. The simulation results of all these experiments are summarized in Figure 5.18. The x-axis denotes the number of test devices in the simulation. The ratio between the training devices and test devices for all the points in the figure is the same as we used in the simulation of section 5.6.2. The y-axis is the correlation coefficient between the estimated THD and the reference THD of the test devices. One can observe that as the number of training devices increases the correlation coefficient also becomes larger. The larger the correlation coefficient is, the more accurate the estimated results are. It is very obvious that the accuracy of the estimated results from 63 training devices is far away from the one based on 2000 training devices. From the simulations one can conclude that if one wants to obtain the same or even better accuracy of the estimated dynamic parameters, 2000 or even more training devices are required. However, more devices are still required in the measurement to confirm this conclusion. One can also observe that the curve in Figure 5.18 becomes gradually flat as the training devices increases from 250 to 2500. If the number of training devices increases to 2500, the correlation coefficient is 0.993. Hence, one can increase the number of training devices for obtaining more accurate estimated results. However, if the number of devices increase from 2000 to 2500 or even more, it can not improve the accuracy of estimation too much but it will increase the computational time.

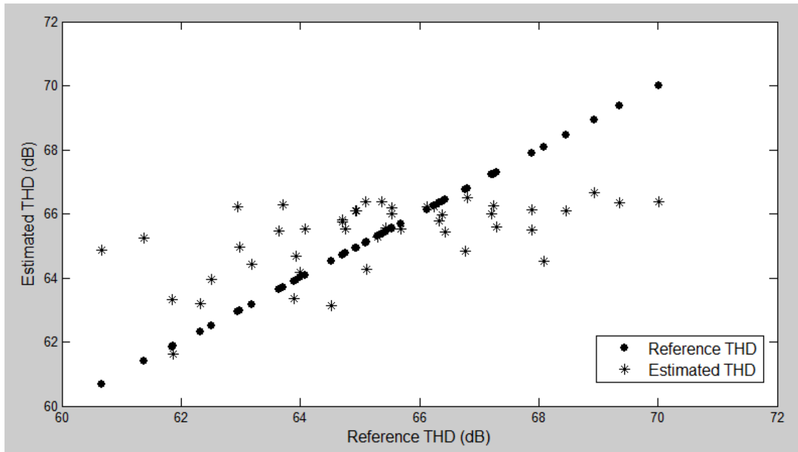

Figure 5.17: The estimated results of the THD in the case of simulation with 63 training devices

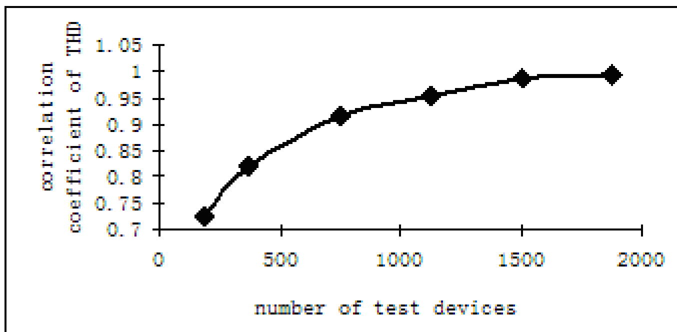

Figure 5.18: The correlation coefficient of the THD of the test devices vs. number of test devices

5.7.2 Measurement results and analysis of the *static* parameters of a 12-bit pipelined ADC

The measurement results of the INL and DNL of the 12-bit pipelined ADCs are shown in Figures 5.19 and 5.20 respectively. The black dots denote the reference results obtained from

conventional testing, while the stars represent the estimated results by our proposed method. The two straight lines are the reference results plus or minus the 3-sigma, which can be seen as the tolerance band of the estimated results. One can observe that although the estimated INL is all in the tolerance band, the correlation between the estimated and reference results is very poor, which is only 0.055. The results of DNL in Figure 5.20 show a better correlation between the reference and estimated results, which is 0.66. However, it is still not sufficient to give accurate estimated results.

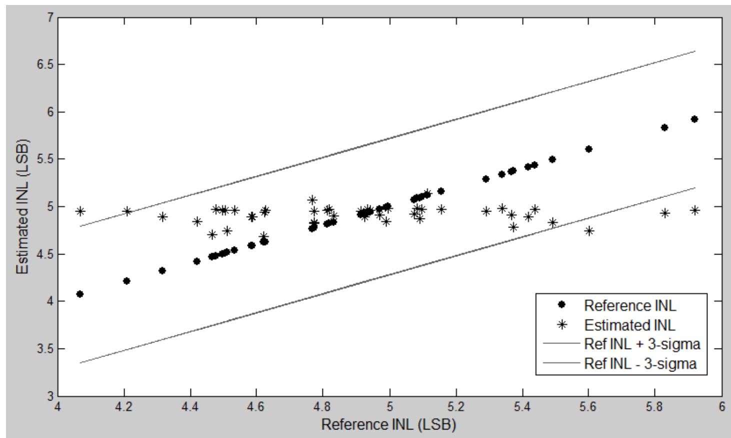

Figure 5.19: The estimated results of the INL with input *pulse 5*

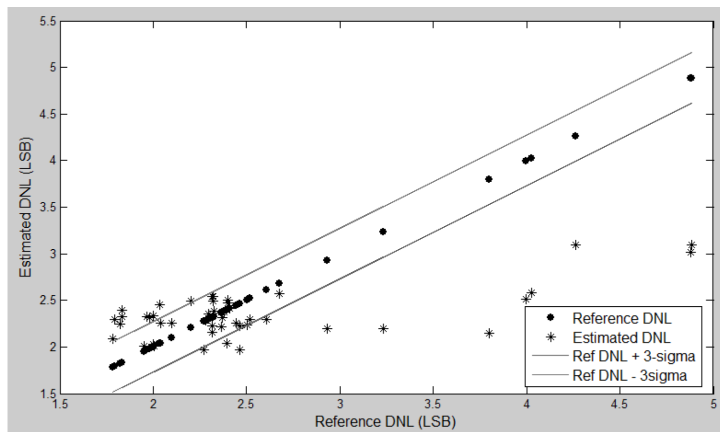

Figure 5.20: The estimated results of the DNL with input *pulse 5*

The measurement results of INL and DNL obtained from the five different pulse waves are summarized in Table 5.9. One can see that there are a significant number of outliers for both the results of the INL and DNL. It is as we expected from Figures 5.19 and 5.20. Therefore, for both simulation and measurement results, we can come to the same conclusion that the proposed method cannot predict the INL and DNL.

Table 5.9: The mean error and outliers in the estimated static results with different standard deviation of the noise of the input signal in measurements

		INL	DNL
Pulse 1	Mean error (dB)	0.45	0.48
	Number of outliers	9	23
Pulse 2	Mean error (dB)	0.47	0.46
	Number of outliers	8	25
Pulse 3	Mean error (dB)	0.43	0.47
	Number of outliers	8	24
Pulse 4	Mean error (dB)	0.43	0.42
	Number of outliers	9	22
Pulse 5	Mean error (dB)	0.33	0.42
	Number of outliers	5	21

5.8 Conclusions

In this chapter, a new machine-learning-based testing approach for ADCs has been proposed, which predicts both the static and dynamic specifications from the signature *ORP*. In order to build the mapping function for prediction, both the specification testing and the signature testing have been carried out on a training set. During mass-production testing only signature-based testing is required for the DUTs, of which the data-processing consumes less computational time than the conventional FFT analysis. In the signature test approach, a noisy and nonlinear pulse wave has been applied as test stimulus. Such a signal is easier and less expensive to generate than a high-quality analogue sine wave as used in the conventional

specification-based testing; this is especially true if the ADCs are integrated into a platform-based design. Therefore, it is suitable to be implemented in a multi-site test environment, which can reduce the test time efficiently.

In order to validate our method, a 12-bit pipelined ADC, modeled in Labview, has been selected as the test vehicle. While test simulating the dynamic parameters, the results show that a pulse wave input stimulus with 7-bit nonlinear edges and an additive noise of 3 LSB standard deviation can obtain accurate estimations of the SFDR, THD and SINAD. Although there are still some outliers in the results, their number does not exceed 3% of the total number of DUTs. In order to validate whether the proposed method can distinguish the faulty devices from correct ones or not, the test sets including faulty ADCs have also been randomly generated by the Labview model. It shows that as the values of the dynamic parameters are more close to the fault-free range, it has a higher possibility to misclassify the DUTs by the proposed method. However, the results show that most of the faulty devices can be detected correctly by the machine-learning-based test method. For testing the static parameters INL and DNL, the estimated results contain too many outliers, which is not acceptable. Therefore, the simulation results show that the proposed method is not suitable for testing the INL and DNL.

The simulation results also show that the machine-learning-based test method has limitations to predict the SNR accurately. We have proposed a method, used before for improving conventional specification-based testing, which has then been applied to our machine-learning-based method. A double-period output waveform is reorganized. By calculating the difference of the two-period output and the differential of the output between two ADCs, the noise induced by the input stimulus can be decreased at the output. The recalculated noise of the output is used as an additional variable for the previous machine-learning-based method. As a result, the accuracy of the SNR prediction can be improved. In the machine-learning-based test, the more the variables are correlated to the specifications the more accurate prediction results will be obtained. Compared with the original double-ADC method, this work applies a pulse-wave instead of a sine wave and uses the machine-learning-based method, which obtains much better accuracy. However, more improvements are still required if it is to be implemented in production testing.

A 12-bit pipelined ADC has been used to validate the method by measurements. From the measurement results, one can see that the proposed method can not predict the static parameters as there is poor correlation between the predicted static parameters and the reference static parameters. This is in line with the simulation results.

For the dynamic parameters, the measurement results show a poor correlation between the estimated dynamic parameters and the reference dynamic parameters. As a result, a lot of outliers exist in the estimated results. This is in contradiction with the simulation results. Compared with the simulations, the most important difference is that there are much more training devices in the simulation than in the measurements. As there were only a limited number of devices during the measurements, we have only verified it in the simulations that the accuracy of the estimated results from 64 training devices are much less accurate than the ones obtained from 2000 training devices. At least 2000 training devices are required if one wants to achieve the same accuracy of the estimated results in our simulation. However, more devices are still required in the measurement to confirm it this in the future.

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Chapter 6

Conclusions and Recommendations

6.1 Conclusions

The objective of this thesis is to find a solution to cut down the production test cost of ADCs by using embedded digital processors. The conventional ADC production testing is a specification-based testing approach, including both static and dynamic testing. Compared with the structural-based testing for digital circuits, it is a very complex task.

Currently, the platform-based designs are very popular, especially for communication, audio and video systems. These designs often contain standard IPs, like mixed-signal circuits, digital processors and memory. In this case, using embedded digital processors to reduce the test cost of ADCs is a very promising solution.

An architecture of an ADC test infrastructure in a platform-based design is proposed in *chapter 2*, consisting of the embedded digital processors, the ADC(s) under test, aiding digital test stimuli circuits and memory. The embedded processor can generate the test input signal with the help of additional circuits and post-processing of the output data. The aiding

circuits adapt the common digital test input stimulus from the processor to be more suitable for ADC testing. The memory stores the conversion output data. In this thesis, we basically proposed three novel methods based on the new architecture:

- Testing of dynamic parameters by using adaptive pulse-wave input stimuli
- Provide a pre-test in a multi-site test environment by using the adaptive pulse-wave input stimulus
- Predict the key test parameters of an ADC by using the adaptive pulse-wave input stimuli based on the MARS algorithm

6.1.1 Testing of dynamic parameters using adaptive pulse-wave input stimuli

In *chapter 3*, pulse waves are exploited as the test input stimulus by emulating the spectrum of a sine wave, which is the conventional test stimulus for dynamic testing. It is emulated in two ways: one is changing the duty cycle and the other is using a stair-case input signal. As the spectrum of a pulse wave is related to its duty cycle, a number of pulse waves with different duty cycles are combined to obtain a similar output spectrum of a sine wave. A sine wave can also be considered as a stair-case signal with countless levels. Hence, increasing the number of voltage levels of a pulse wave will also be a way to emulate the spectrum of a sine wave. For the post-processing, the conventional FFT analysis is exploited to obtain dynamic test results. These results show that the dynamic parameters obtained by a pulse wave signal are not as accurate as the ones obtained by a sine wave. However, they have the same trend. In this case, the results obtained by a pulse wave can be used to reflect the faults in the DUTs. The simulation of the methods is carried out at both the transistor-level netlist of a 6-bit flash ADC as well as the Labview model of a 12-bit pipelined ADC. The measurements are carried out on a 12-bit pipelined ADC corresponding to the Labview model. Both the simulation and measurement results indicate that the pulse wave with different duty cycles is more sensitive to the faults in the ADCs than the stair-case signal. They can successively filter out the faulty devices before the DUTs proceed to the conventional production testing.

6.1.2 A pre-test in a multi-site test environment by using a digital input stimulus

In *chapter 4*, a simple pulse wave is investigated as the test stimulus. For post-processing, an unconventional method is exploited that by comparing the similarity of the output signature between the golden devices and the DUTs, a fault classification can be provided. As the test stimulus is easy to generate and the post-processing is also simple, it is suitable to be applied in a multi-site test environment. Hence, it can be a fast and simple pre-test to filter out the faulty devices. For the post-processing, we propose three different methods based on a similar idea. They are the comparison of the output in terms of amplitude, angle and frequency respectively. The 6-bit flash ADC and the 12-bit pipelined ADC in *chapter 3* are still exploited to validate the methods in simulation. The 12-bit pipelined ADC is the DUT being used in the measurements. Different number of samples and a variation of the edges are also applied to investigate if the methods are strongly affected by them. The impact of the starting sampling point is also studied on the measurement results. It shows that if the starting sampling point changes for both golden devices and DUTs, the proposed method can still distinguish the faulty devices. Both the simulation and measurement results indicate that the method with a comparison in terms of amplitude is the most robust; it can detect all faults and is not sensitive to different setups in number of samples or jitter.

6.1.3 Prediction of the dynamic and static specifications of an ADC with a low-quality digital input stimulus

In *chapter 5*, a machine-learning-based test method is proposed to predict the specifications of the ADCs. A low-quality digital pulse wave is applied as the test stimulus. By collecting the training data, which contains both the specification and the signature results of the training devices, a mapping function is built up between the specifications and signature results. While testing the DUTs, only the signature testing by using the pulse wave is required. Finally, the specifications of the DUTs can be predicted by substituting the signature results into the mapping function. In this method, the principle of the signature testing is similar as the pre-test proposed in *chapter 4*. As a result, it is a simple and fast signature testing compared with the conventional dynamic testing. In this case, it can reduce

the test time of the DUTs. Both the simulations and the measurements are carried out on a 12-bit pipelined ADC. The simulation results show that a pulse wave input stimulus with 7-bit nonlinear edges and an additive noise of 3 LSB standard deviation can obtain accurate estimations of the SFDR, THD and SINAD. For the static parameters INL and DNL, the simulation results show that the estimations are not sufficiently accurate. The method also has limitations with respect to predict the SNR accurately. In this case, an improved method is proposed based on the existing double-ADC method. The simulation results indicate that it improves the accuracy of the SNR prediction. In the measurement results, one can see that INL can not be predicted by the proposed method, which matches the simulation results. The estimated DNL in the measurement shows the correlation with the reference DNL. But the correlation coefficient of the DNL is still far away from an acceptable value. The measurement results of all the dynamic parameters show a poor correlation between the estimated results and the reference values. This is not matched with the simulation results. The major difference between the simulations and the measurements is the number of training devices. As the number of devices is limited, we only verified it in simulation that the correlation becomes poor in the case the number of training devices decreases. In future, this problem can be investigated in more detail if more devices become available.

6.1.4 Overall conclusion

Summarizing, our proposed test infrastructure of the ADCs integrated into a platform-based design can be built by using an embedded digital processor and associated memory. Based on the test infrastructure, either signature results are used to only filter out the faulty devices or accurately predicted dynamic results of the ADCs can be obtained. Both the test input signal generation as well as post-processing can be carried out on the embedded processor. In this way, it relaxes the requirement of the ATE, which is normally the bottleneck in ADC production testing. It is especially suitable for a multi-site test environment. As result, it can reduce the test time and cost of ADC production testing.

Our major contributions proposed in this thesis are as follows:

- A test approach has been proposed using the pulse-wave input stimulus of different duty cycles, which can emulate the spectrum of a sine wave and reflect the faults in the ADCs.
- A pre-test method has been presented using a pulse wave as the test stimulus and the

out-of-range percentage to process the output data, which can filter out the faulty ADCs before going through the complex conventional ADC testing.

- A machine- learning based test method using a low- quality pulse wave as the test stimulus has been proposed, which can predict the dynamic parameters of the ADCs accurately in simulation. The validation in terms of measurements with more devices is still required in the future.

6.2 Recommendations for further research

The main recommendations for future research in the area of testing ADC by using digital stimuli are the following:

- The methods in this thesis are only validated via simulation or measurement of the 6-bit flash ADC and the 12-bit pipelined ADC. Other types of ADCs should be applied to investigate the proposed test methods in the future.
- In the measurements, the faulty devices are not available but only emulated by the fault-free devices. The measurement of the proposed methods on real faulty devices can be carried out in the future
- In the machine-learning-based test methods, the number of devices in the measurements is limited. As the method is based on statistics theory, the measurements should be carried out on much more devices to evaluate the proposed method.
- In the machine-learning-based test methods, the outliers are always a problem. In the future, the method for distinguishing or decreasing the outliers should be investigated.
- In the thesis, the dynamic parameters of the ADCs can be obtained by using the proposed test infrastructure. However, the static results are not sufficiently accurate. In the future, the test method with respect to the ADC static specifications based on the proposed BIST structure should be investigated.
- A real platform-based design can be selected as a prototype to implement the proposed methods in the thesis, although this has started based on a FPGA.

6.3 List of publications

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Summary

The Analogue-to-Digital Converter (ADC) is one of the most typical and widely used mixed-signal circuits. They are applied in video, audio, high-speed communications systems and so on. Many ADCs are integrated into platform-based designs, the architecture which normally contains of standard blocks such as memories, digital processors, RF and analogue front-ends. As testing such a system is a complex task, the related test cost of the platforms is a major part of over all chip costs. The test cost of ADCs has a relatively high percentage of the total test cost of the chips. The major challenges of the ADC production test cost are the expensive test equipment and the long test times.

An architecture of an ADC test infrastructure in a platform-based design has been proposed in our research, which consists of the embedded digital processor(s), the ADC under test, aiding digital test stimuli circuits and memory. The embedded processor can generate the test input signal with the aiding circuits and post-process the output data. The aiding circuits adapt the normal digital signal from the processors to be more suitable for ADC testing. The memory can store the conversion output data. In this thesis, we basically propose three novel methods.

The first method is using the adaptive pulse wave to test the dynamic parameters. In this method, a number of pulse waves with different duty cycles are applied to the ADC under test as the test stimulus. As the spectrum of a pulse wave is related to its duty cycle, the spectrum of a sine wave is emulated by the spectrum of a number of pulse waves with different duty cycles. In this way, the dynamic parameters of the ADC under test can be calculated. The results can be used to filter out the faulty devices before the ADC under test proceeds to the conventional production testing.

In the second method, only a simple pulse wave is applied as the test stimulus. In the post-processing, an unconventional method has been proposed. Signature results are obtained by comparing the similarity of the output waveforms between the golden devices and the device under test (DUT). The signature results can classify the faulty device and the

fault-free devices. As the test stimulus is easy to generate and the post-processing is simple, it is very suitable to apply in a multi-site test environment. The method has been proposed as a quick pre-test to filter out the faulty devices before the conventional production test of DUTs.

In the case of the third method, a machine-learning based test method to predict the dynamic parameters of the ADCs has been proposed. A low-quality pulse wave is exploited as the test stimulus. The signature test is carried out by applying the pulse wave input signal. For the training devices, both the signature test and conventional specification tests are carried out. A mapping function can be built up between the signature results and the specification results. For the DUTs, only a signature test is required. Afterwards, the specification results of the DUTs can be predicted by substituting the signature results to the mapping function. As the signature test is simple and suitable for multi-site test, the proposed test method can reduce the test time compared with the conventional test.

Summarizing, based on our proposed test infrastructure, either signature results are used to only filter out the faulty devices or accurately predicted dynamic results of the ADCs can be obtained. Both the test input signal generation and post-processing can be carried out on the embedded processor. In this way, it relaxes the requirements of the ATE, which is normally the bottleneck in ADC production testing. It is especially suitable for a multi-site test environment. As result, it can reduce the test time and the cost of ADC production testing.

Abbreviations

ADC	Analogue-to-Digital Converter
ATE	Automatic Test Equipment
AWG	Arbitrary Waveform Generator
BIST	Built-In Self Test
DAC	Digital-to-Analogue Converter
DIB	Device Interface Boards
DNL	Differential Non-Linearity
DUT	Devices-under-Test DUT
ENOB	Effective Number of Bits
FFT	Fast Fourier transform
IC	Integrated Circuit
INL	Integral Non-Linearity
IO	Input / Output Interface
LSB	Least Significant Bit
MARS	Multivariate Adaptive Regression Splines
MDAC	Multiplying Digital-to-Analogue Converter
ORP	Out-of-Range Percentage
PLL	Phase-Locked Loop
PWM	Pulse-Width Modulated
RF	Radio- Frequency
SEIR	Stimulus Error Identification and

Removal

SFDR	Spurious Free Dynamic Range
SINAD	Signal-to-Noise-and-Distortion
SNR	Signal-to-Noise Ratio
SoC	System-on-Chip
THD	Total Harmonic Distortion
TSR	Ternary Signal Representation

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Biography

Xiaoqin Sheng was born on June 4th 1981, in Wuhan, China. She obtained her B.Sc. degree in Electrical Communication Engineering from Huazhong University of Science and Technology, Wuhan, China in 2003. She received her M.Sc. degree in Electrical Engineering from Linköping University, Sweden in 2005. In the same year, she joined O2 Micro, Wuhan, China as an analog electronic designer. In 2006, she became a PhD candidate in the CAES-TDT group at the University of Twente, the Netherlands. During her PhD study, her research interest was mixed-signal testing. Currently she is a test architect at Melexis Semiconductors in Belgium.